VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Analog Electronic Circuits			
Course Code	**21EC34**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Teaching-Learning Process (General Instructions)
These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1.Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2.Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4.Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5.Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6.Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7.Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. **RBT Level:** L1, L2, L3

Module-2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low

frequency response. **Oscillators:** FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. **RBT Level:** L1, L2, L3
Module-3	
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Class D power amplifier. **RBT Level:** L1, L2, L3
Module-4	
Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Clippers and Clampers, Peak detector, Sample and hold circuit. **RBT Level:** L1, L2, L3
Module-5	
Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2, 2.3, 2.4,2.6, 2.7,2.9, 2.10, 3.2, 3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. **RBT Level:** L1, L2, L3
Course Outcomes (Course Skill Set) At the end of the course the student will be able to : 1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits. 2. Design and analyze FET amplifiers and oscillators with different circuit configurations and biasing conditions. 3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators. 4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers. 5. Understand the power electronic device components and its functions for basic power electronic circuits.	

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015. ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. Electronic Principles, Albert Malvino, David J Bates, 7th Edition, McGraw Hill Education (India) Private Limited, 2017, ISBN:978-0-07-063424-4

Web links and Video Lectures (e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

A E C

21EC34

Module-1

Analog Electronics Circuits

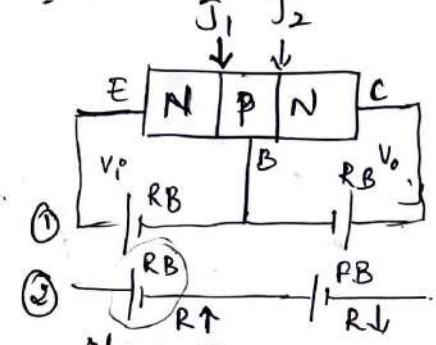
→ Simple form of switch in electronics is a diode.

ON ⇒ Forward biased OFF ⇒ Reverse biased.

→ Advance Version ⇒ transistor → It is 3 terminal device (Emitter, Base, Collector)
→ is used to amplify a weak signal
→ two types → NPN → commonly used
→ PNP.

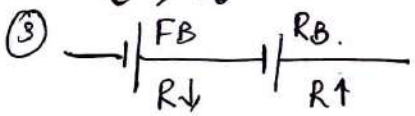
→ BJT
↓ ↓ ↓
Bipolar Junction transistors.

V=I(R) two junctions.

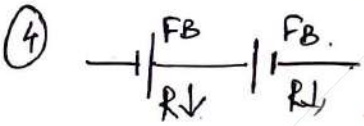


∵ V=IR.

Vi > Vo



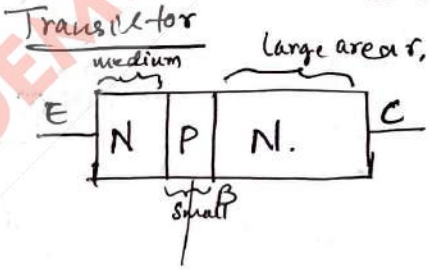
Vo > Vi → Amplifier.



Vo = Vi

	J1	J2		
①	RB	RB	Vo = 0 (Vi > Vo)	Cut off → OFF region
②	RB	FB	→ Attenuation.	
③	FB	RB	Vo > Vi	→ active Region
④	FB	FB	Vo = Vi	→ Saturation (ON) Region

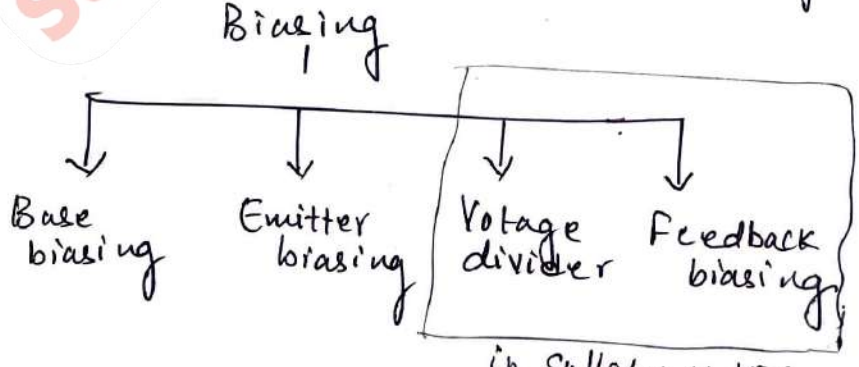
two turn ON & OFF we cannot use diode itself thats why we will use ③ condition.



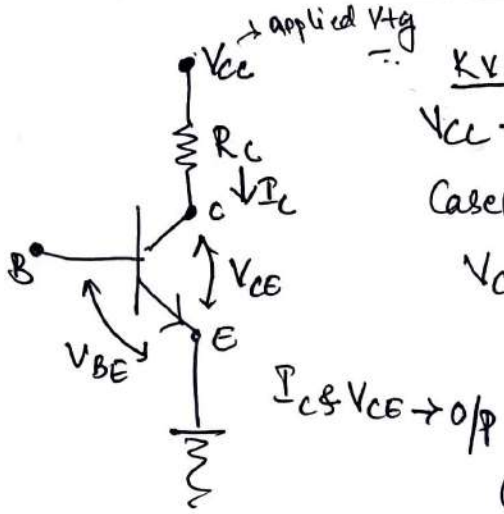
	area	doping
C	large	MODERATE
E	medium	HIGH
B	small	LIGHTLY

Biasing → Appropriate Voltage applied to device to turn ON.

[Ex: Charging your mobile with 5V & 1A/2A current.]
↳ biasing Voltage.



in Syllabus of VTU.



simple transistor circuit.

I_C & V_{CE} → o/p

∴ KVL

$V_{CC} - I_C R_C - V_{CE} = 0$

Case (i) take $I_{C_{max}}$ $V_{CE} = 0$.

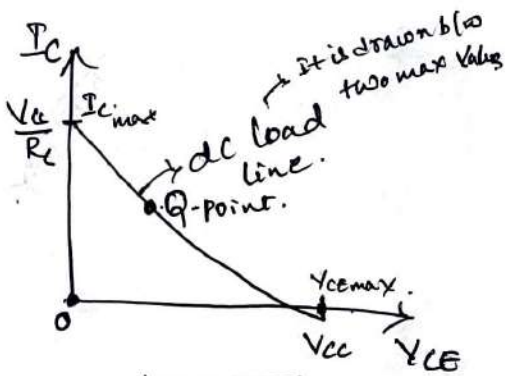
$V_{CC} - I_{C_{max}} R_C = 0$

$$I_{C_{max}} = \frac{V_{CC}}{R_C}$$

Case (i) $V_{CE_{max}}$ $I_C = 0$

$V_{CC} - V_{CE_{max}} = 0$

$$V_{CE\,max} = V_{CC}$$

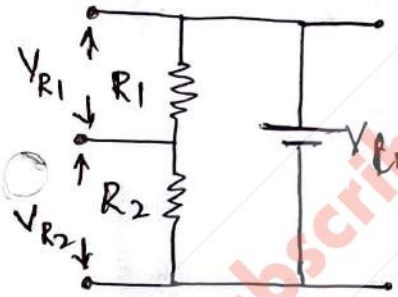


Q-point → center of load line.
operating point.
↳ at operating point
Transistor ⇒ Active Region
↳ act as Amplifier.

→ Hence for biasing $\left(\frac{I_{C_{max}}}{2}, \frac{V_{CE_{max}}}{2}\right)$

(I_{CQ}, V_{CEQ}).

Voltage divider bias Circuit:- dividing voltage for biasing to establish stable operating point.



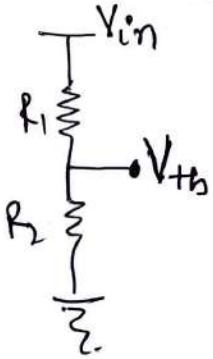
$$V_{R_2} = \frac{R_2}{R_1+R_2} V_{in}$$

$$V_{R_1} = \frac{R_1}{R_1+R_2} V_{in}.$$

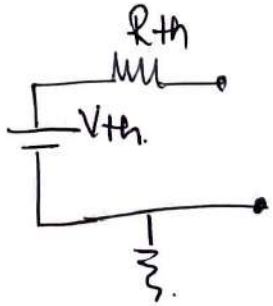
if $R_1 = R_2$ then $V_{R_1} = V_{R_2} = \frac{V_{in}}{2}$

→ Thevenin's theorem.

Step ①



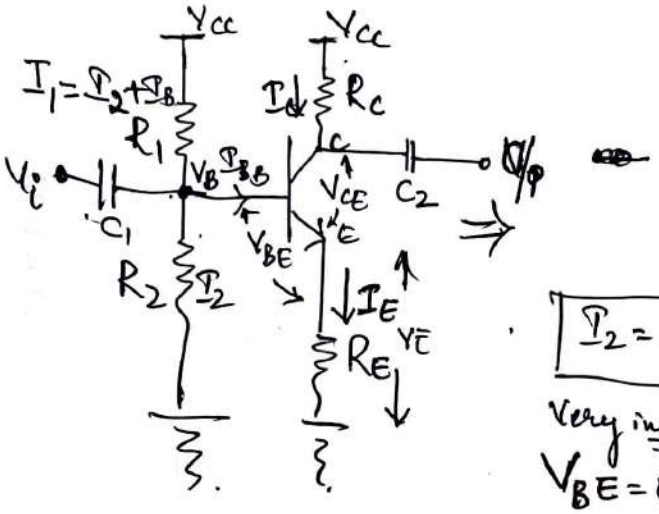
$$V_{th} = \frac{R_2}{R_1+R_2} V_{in}.$$



Step ②

$R_1 || R_2$.

$$R_{th} = \frac{R_1 R_2}{R_1+R_2}$$



$I_2 = 10 I_B$

Very imp for biasing.

$V_{BE} = 0.7$

Voltage divider circuit. ** $V_B = V_{BE} + V_E$

$R_C \rightarrow$ o/p resistance.

$R_E \rightarrow$ Emitter Res. + used for Stability

R_1 & R_2 - Vtg divider bias resistors

C_1 & C_2 - Coupling capacitor

V_{CE} - C to E Vtg

V_E - Emitter Vtg

V_{BE} - B to E Vtg = 0.7

V_B - Base Vtg

I_C - Collector current → o/p current

I_E - Emitter current →

I_B - Base current → i/p current

Current gain = $\frac{\text{Current o/p}}{\text{Current i/p}} = \frac{I_C}{I_B} = \beta$ ** Important.

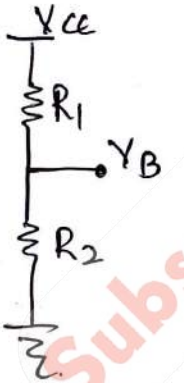
$I_E = I_C + I_B$ **

$\because I_C = \beta I_B$

$I_E = \beta I_B + I_B$

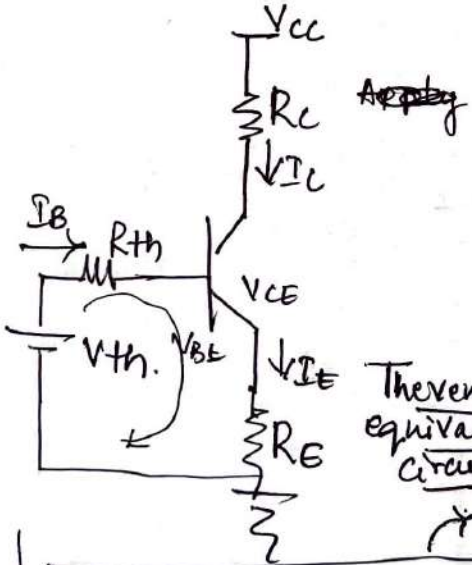
$I_E = I_B(\beta + 1)$ **

** Very imp formula for any transistors.



$V_{th} = \frac{R_2}{R_1 + R_2} V_{cc}$

$R_{th} = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2}$



Apply KVL for i/p side

$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$

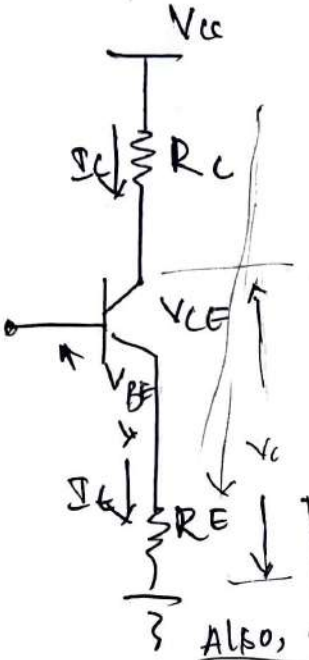
$\because I_E = I_B(1+\beta)$

$V_{th} - I_B R_{th} - V_{BE} - I_B(1+\beta) R_E = 0$

$V_{th} - V_{BE} - I_B [R_{th} + (1+\beta) R_E] = 0$

$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}$

$I_E = \frac{V_{th} - V_{BE}}{R_E + \frac{R_{th}}{(1+\beta)}}$



Apply KVL to o/p side,

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

to find operating point. find I_C & V_{CE}

$$I_C = \frac{V_{CC} - V_{CE} - I_E R_E}{R_C}$$ → o/p current

Voltage divider current = $0.1 I_E$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$ → o/p vtg

Also, To make I_E insensitive to temp & β variations,

$V_{th} \gg V_{BE}$ and $R_E \gg \frac{R_B}{1+\beta}$ → Also to provide large vtg swing & $V_{CE} = I_C R_C = 1/3 V_{CC}$

$V_B = V_{th} = 1/3 V_{CC}$ & specifications

Problem

Design a Vtg divider biasing for the BJT with $V_{CC} = +12V$, $I_E = 1mA$, $\beta = 100$.

$V_B = V_{th} = \frac{1}{3} V_{CC} = \frac{1}{3} \times 12 \Rightarrow V_{th} = 4V = V_B$

$V_B = V_{BE} + V_E \Rightarrow V_E = V_B - V_{BE} = 4 - 0.7 \Rightarrow V_E = 3.3V$

$R_E = \frac{V_E}{I_E} = \frac{3.3}{1m} \Rightarrow R_E = 3.3K\Omega$

Voltage divider current = $0.1 I_E = 0.1 \times 1m = 0.1mA$

$R_1 + R_2 = \frac{12}{0.1m} = 120K\Omega$.

$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{80K \times 40K}{80K + 40K} \Rightarrow R_{th} = 26.67\Omega$

$V_{th} = \frac{R_2}{R_1 + R_2} V_{CC} \Rightarrow 4 = \frac{R_2}{R_1 + R_2} \times 12 \Rightarrow 4 = \frac{R_2}{120K} \times 12$

$\Rightarrow R_2 = 40K\Omega$

$R_1 + 40K = 120K \Rightarrow R_1 = 80K\Omega$

$\therefore I_E = \frac{V_{th} - V_{BE}}{R_E + R_{th}/(1+\beta)} = \frac{4 - 0.7}{3.3K + \frac{26.67}{101}} = 0.99 \times 10^{-3} A$

$I_E \cong 1mA$

$\alpha = \frac{\beta}{\beta - 1} \Rightarrow \alpha = \frac{100}{100-1}$

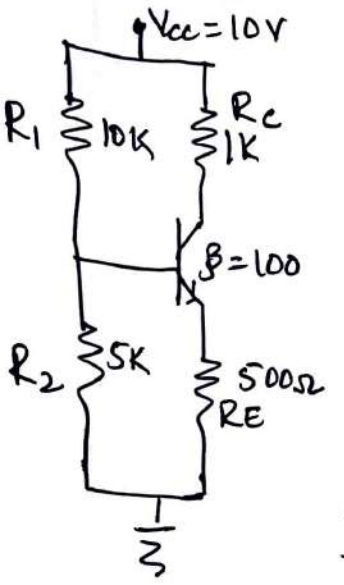
$\alpha = 0.99$

$R_C = \frac{V_{CC} - V_C}{I_C}$ $I_C R_C = 1/3 V_{CC}$

$R_C = \frac{4}{1mA} \Rightarrow R_C = 4K\Omega$ $I_C = 0.99 I_E \Rightarrow 0.99mA$

$I_C = 1mA$

Problem: (2) Calculate V_{CE} & I_C for Below circuit.



$$I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$V_{th} = \frac{R_2}{R_1+R_2} \cdot V_{cc} = \frac{5K}{10K+5K} \times 10$$

$$\boxed{V_{th} = 3.33V}$$

$$I_B = \frac{3.33 - 0.7}{3.33K + (101)500}$$

$$R_B = R_{th} = \frac{R_1 R_2}{R_1+R_2} = \frac{5\times10}{5+10}$$

$$\boxed{I_B = 48.864\mu A}$$

$$\boxed{R_B = R_{th} = 3.33K\Omega}$$

$$I_C = \frac{V_{cc} - V_{CE} - I_E R_E}{R_E}$$

$$I_C = \beta I_B$$

$$I_C = 100 \times 48.864$$

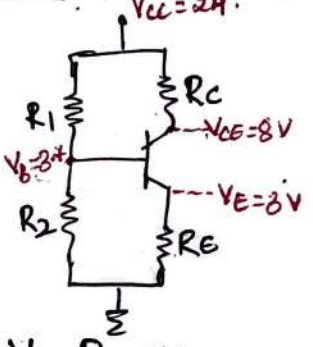
$$\boxed{I_C = 4.886mA}$$

$$I_E = (1+\beta)I_B = 101 \times 48.864 \Rightarrow \boxed{I_E = 4.036mA}$$

$$V_{CE} = V_{cc} - I_C R_C - I_E R_E$$

$$= 10 - 4.86\times10^{-3}\times1\times10^{3} - 4.03\times10^{-3}\times500$$

$$\boxed{V_{CE} = 2.64V}$$



(3) Design Vtg divider bias using supply of 24V, $\beta = 110$; (Find resistance value.)

$I_C = 4mA$, $V_{CEQ} = 8V$, $V_E = \frac{V_{cc}}{8}$.

(1) Find currents.

$I_C = 4mA$.

$$I_B = \frac{I_C}{\beta} = \frac{4m}{110} \Rightarrow \boxed{I_B = 36.364\mu A}$$

$$I_E = (1+\beta)I_B = (111)\,36.364\mu A$$

$$\boxed{I_E = 4.036mA}$$

$$I_2 = 10 I_B = 10\times36.364\mu A$$

$$\boxed{I_2 = 360.364\mu A}$$

$$\boxed{I_1 = I_2 + I_B = 360.36 + 36.36 = 396\mu A}$$

(2) Find Vtgs

$\boxed{V_{BE} = 0.7V}$, $V_{CE} = 8V$, $V_{cc} = 24V$

$$V_E = \frac{24}{8} \Rightarrow \boxed{V_E = 3V}$$

$$V_B = V_{BE} + V_E = 0.7 + 3V \Rightarrow \boxed{V_B = 3.7V}$$

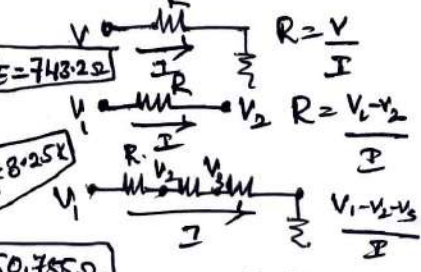
(3) Find Resistance

$$R_E = \frac{V_E}{I_E} = \frac{3}{4.036m} \Rightarrow \boxed{R_E = 743.2\Omega}$$

$$R_C = \frac{24 - 8 - 3}{4mA} \Rightarrow \boxed{R_C = 8.25K}$$

$$R_1 = \frac{24 - 3.7}{396\mu} \Rightarrow \boxed{R_1 = 50.755K\Omega}$$

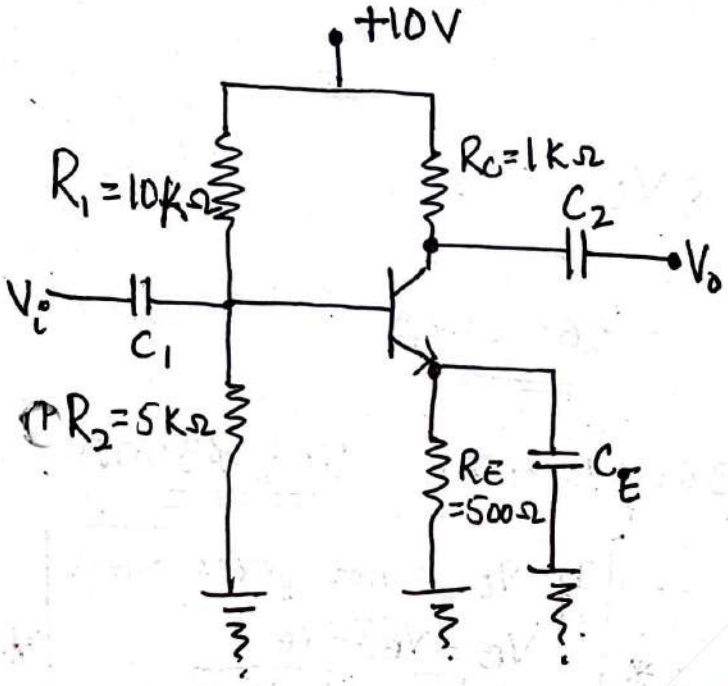
$$R_2 = \frac{3.7}{360.364\mu} \Rightarrow \boxed{R_2 = 10.176K\Omega}$$



Voltage divider bias

Problems :

(1) For the circuit shown in figure, $\beta = 100$ for Silicon transistor. Calculate V_{CE} and I_C



$$V_{Th} = \frac{R_2}{R_1+R_2} V_{CC} = \frac{5\times10^3}{10\times10^3+5\times10^3}$$

$$\boxed{V_{th} = 3.33\,V}$$

$$R_{Th} = R_B = \frac{R_1 R_2}{R_1+R_2} = \frac{10\times5}{10+5}$$

$$\boxed{R_{th} = 3.33\,K\Omega}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{3.33 - 0.7}{3.3K + (101)500}$$

$$\boxed{I_B = 48.86\,\mu A}$$

$$I_C = \beta I_B \Rightarrow I_C = 100 \times 48.86\mu \Rightarrow \boxed{I_C = 4.886\,mA}$$

$$I_E = I_C \Rightarrow \boxed{I_E = 4.886\,mA}$$

$$I_E = (\beta+1) I_B = 101 \times 48.86\mu$$

$$\boxed{I_E = 4.934\,mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = 10 - (4.886m \times 1K) - [4.935m \times 500]$$

$$\boxed{V_{CE} = 2.6465\,V}$$

(2) Design a voltage divider bias n/w using a supply of 24V, $\beta = 110$ and $I_{CQ} = 4mA$, $V_{CEQ} = 8V$. $V_E = V_{CC}/8$.

Soln :- Given $I_{CQ} = 4mA$, $V_{CEQ} = 8V$, $V_E = V_{CC}/8 = 3V$, $V_{CC} = 24V$, $\beta = 110$.

Step 1 :- Obtain I_B, I_E & V_E

$$I_B = \frac{I_{CQ}}{\beta} = \frac{4mA}{110} = 36.364\mu A$$

$\because I_C = \beta I_B$

$$I_E = I_B + I_C = 36.364\mu + 4m = 4.0363mA$$

$$V_E = \frac{V_{CC}}{8} = \frac{24}{8} = 3V$$

** If V_E is not given, then
$V_B = V_{BE} + V_E$
$\Rightarrow V_E = V_B - V_{BE}$
$V_B = V_{th} = V_3 V_{CC}$ *

Step 2 :- Obtain R_E & R_C

$$R_E = \frac{V_E}{I_E} = \frac{3}{4.0363m} \Rightarrow R_E = 743.24\Omega$$

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{24 - 8 - 3}{4m} \Rightarrow$$

$$R_C = 3.25K\Omega$$

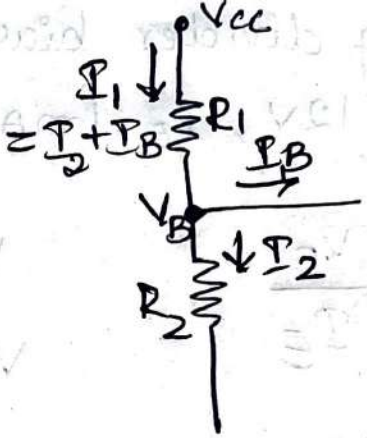
Step 3 :- Obtain R_1 & R_2

$$V_B = V_E + V_{BE} = 3 + 0.7$$

$$V_B = 3.7V$$

$I_2 = 10 I_B = 10 \times 36.364$

$I_2 = 363.64 A$

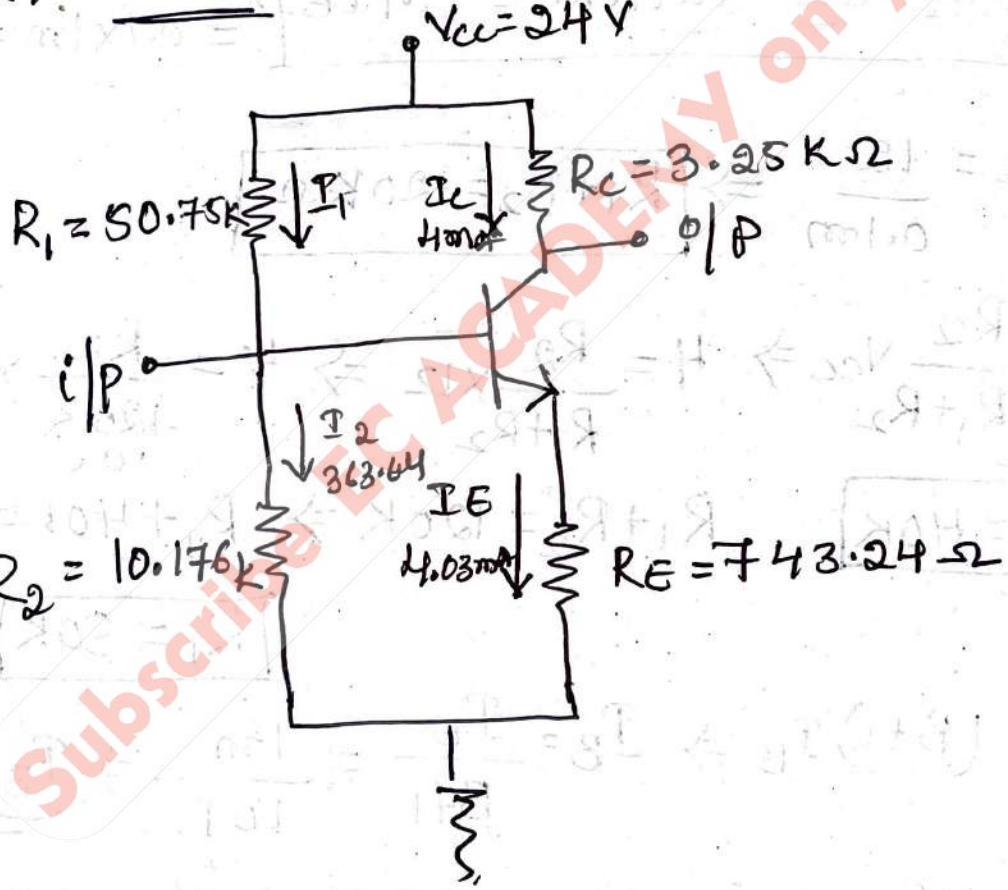


$R_2 = \frac{V_B}{I_2} = \frac{3.7}{363.64}$

$R_2 = 10.176 K\Omega$

$R_1 = \frac{V_{cc} - V_B}{I_2 + I_B} = \frac{24 - 3.7}{(363.64 + 36.364)}$

$R_1 = 50.755 K\Omega$



③ Design a Vtg divider biasing for the BJT specifications with $V_{CC} = 12V$, $I_E = 1mA$ & $\beta = 100$.

Soln:-

$R_E = \frac{V_E}{I_E}$

$R_E = \frac{3.3V}{1m}$

$\boxed{R_E = 3.3K\Omega}$

$V_B = V_{BE} + V_E$

$V_E = V_B - V_{BE}$

$V_E = 4V - 0.7V$

$\boxed{V_E = 3.3V}$

$V_B = V_{th} = \frac{1}{3} V_{CC}$

$V_B = \frac{1}{3} \times 12$

$\boxed{V_B = 4V}$

** Vltage divider current = $0.1 I_E$ ** $= 0.1 \times 1m = 0.1mA$

$R_1 + R_2 = \frac{12}{0.1m} \Rightarrow \boxed{R_1 + R_2 = 120K\Omega}$

$V_{th} = \frac{R_2}{R_1+R_2} V_{CC} \Rightarrow 4 = \frac{R_2}{R_1+R_2} \times 12 \Rightarrow 4 = \frac{R_2}{120K} \times 12$ (10)

$\boxed{R_2 = 40K}$

$R_1 + R_2 = 120K \Rightarrow R_1 + 40K = 120K$

$\boxed{R_1 = 80K}$

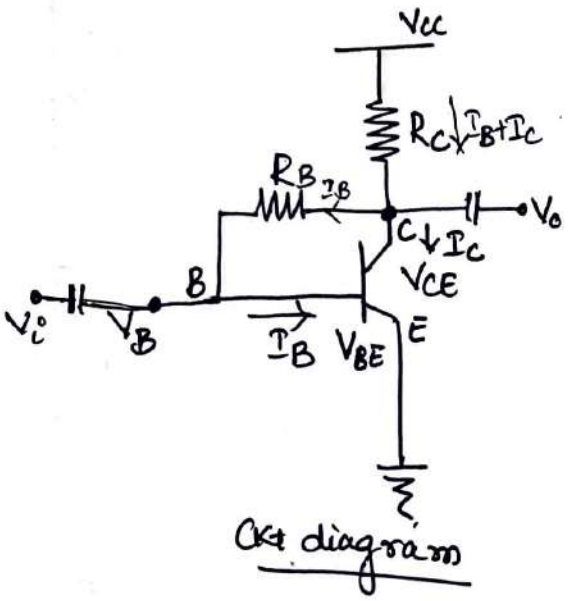
$I_E = (\beta+1) I_B \Rightarrow I_B = \frac{I_E}{\beta+1} = \frac{1m}{101} \Rightarrow I_B = 9.9\mu A$

$I_C = \beta I_B \Rightarrow I_C = 100 \times 9.9\mu \Rightarrow I_C = 0.99mA$

$I_C R_C = \frac{1}{3} V_{CC} \Rightarrow 0.99\mu R_C = 4$

$\Rightarrow \boxed{R_C = 4K\Omega}$

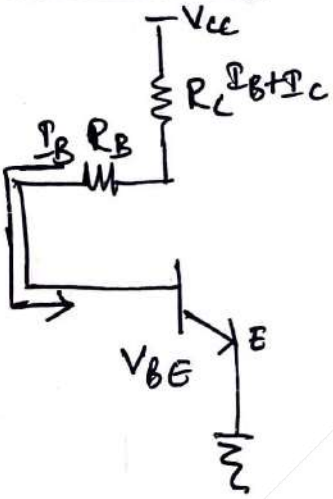
Biasing using Collector to Base feedback



Ckt diagram

R_C → collector Res. | o/p resistance
R_B → Feedback Res | Biasing Res.
C_1 & C_2 → Coupling Capacitor
I_B → Base current
I_C → Collector current
$I_B + I_C$ → current through R_C.
V_{cc} → Power supply
V_{CE} → C to E V+ve
V_{BE} → 0.7 B to E V+ve
V_B → base V+ve

I/p Side



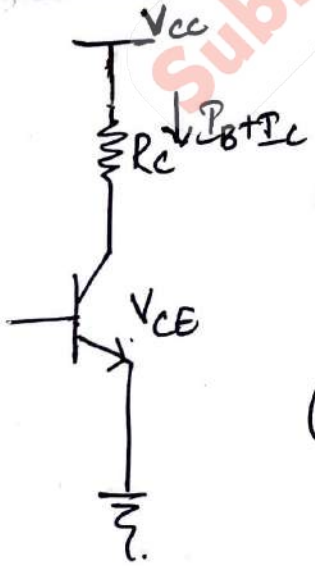
KVL,

$$V_{cc} - [I_B + I_C(R_C)] - I_B R_B - V_{BE} = 0$$

$$V_{cc} - I_B(1+\beta R_C) - I_B R_B - V_{BE} = 0 \quad \because I_C = \beta I_B$$

$$\boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)R_C}} \rightarrow (1)$$

O/p Side



KVL, $I_B(1+\beta R_C)$

$$V_{cc} - (I_B + I_C)R_C - V_{CE} = 0 \rightarrow (2)$$

(i) $$\boxed{V_{CE} = V_{cc} - I_B(1+\beta)R_C} \rightarrow (3)$$

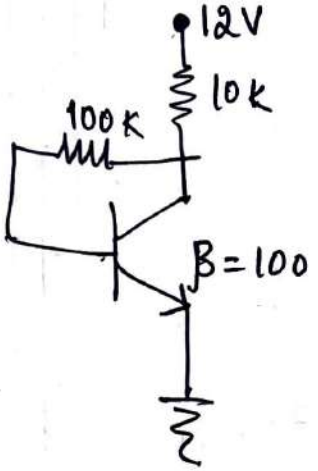
$$\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$$

(2) $\Rightarrow$ $$V_{cc} - \left(\frac{I_C}{\beta} + I_C\right)R_C - V_{CE} = 0$$

$$\boxed{I_C = \frac{V_{cc} - V_{CE}}{(1+1/\beta)R_C}} \rightarrow (4)$$

Problems

① Calculate @ point I_C & V_{CE}.



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} = \frac{12 - 0.7}{100K + (101)10K}$$

$$\boxed{I_B = 10.18\mu A}$$

$$I_C = \beta I_B \Rightarrow 100 \times 10.18\mu A$$

$$\boxed{I_C = 1.018mA}$$

$$V_{CE} = V_{CC} - I_B(1+\beta)R_C$$

$$= 12 - 10.18 \times 10^{-6}(101)10\times10^{3}$$

$$\boxed{V_{CE} = 1.7182V}$$

Q point is at (1.018mA, 1.7182V).

② Design a Collector to base bias circuit for the $V_{CC} = 15V$, $V_{CE} = 5V$, $I_C = 5mA$, $\beta = 100$.

To Find the currents

$I_C = 5mA$

$$I_B = \frac{I_C}{\beta} = \frac{5m}{100} \Rightarrow \boxed{I_B = 50\mu A}$$

$I_E = I_B + I_C = 50\mu + 5m.$

To Find the Volts

$V_{CC} = 15V$ $V_{BE} = 0.7V$

$V_{CE} = 5V$

$V_B =$

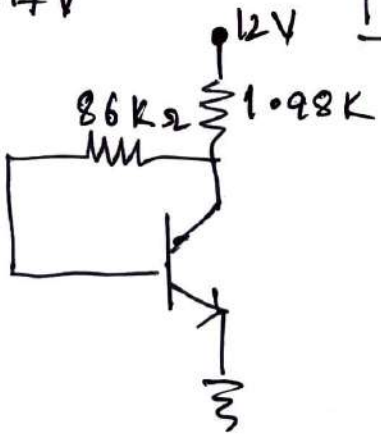
To Find Resistance

$$R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C} = \frac{15 - 5}{50\mu + 5m.}$$

$$\boxed{R_C = 1.98K\Omega}$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{5 - 0.7}{50\mu.}$$

$$\boxed{R_B = 86.K\Omega}$$



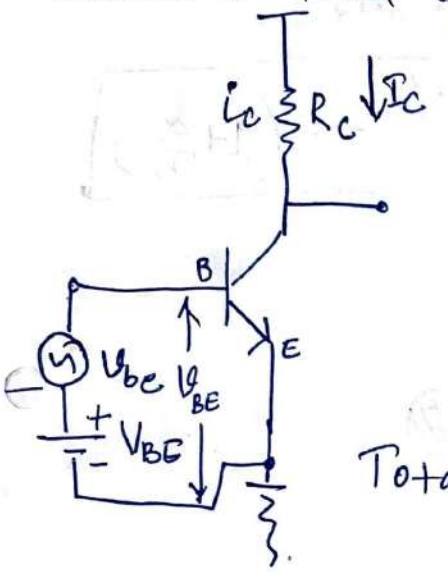
Small signal model (BJT)

→ To operate transistor in active region, it should be biased in active mode; J_{EB} → FB & J_{CB} → RB

→ we will apply both ac & dc signal & small variation occurs in the model.

→ Aim is to find ac current & ac voltage.

ac → Small letters
dc → Capital letters.



3 types of voltage

v_{be} → ac signal
V_{BE} → DC signal
v_{BE} → total signal = ac + dc

Total signal = ac + dc

$$v_{BE} = v_{be} + V_{BE} \longrightarrow (1)$$

3 types of current

I_C → dc signal (current)
i_c → ac Current
i_C → Total Current

$$i_C = i_c + I_C \longrightarrow (2)$$

Total current

from current eqn: $I = I_S (e^{V/V_T})$ →

$$I_C = I_S (e^{V_{BE}/V_T}) \longrightarrow (3)$$

I_S → Secondary current
V_{BE} → dc Vtg
V_T → Thermal Vtg
$V_T = 0.26mV$
I_C → Collector Current

Total current $i_C = I_S (e^{v_{BE}/V_T}) \rightarrow (4)$

$$\boxed{i_C = I_S \left(e^{(v_{be}+V_{BE})/V_T}\right)}$$

put eqn (1) in (4)

$$\because \boxed{e^{a+b} = e^a + e^b}$$

$$i_C = I_S \left(e^{v_{be}/V_T} \cdot e^{V_{BE}/V_T}\right) \rightarrow (5)$$

I_S small ac current; e^{V_{BE}/V_T} small dc current

$$i_C = I_C e^{v_{be}/V_T}$$

$$\boxed{e^{a/b} = \cdots \left(1 + \frac{a}{b}\right)}$$

$$i_C = I_C \left(1 + \frac{v_{be}}{V_T}\right)$$

i_C total current; I_C DC using eqn (3); $\left(1 + \frac{v_{be}}{V_T}\right)$ using eqn (2)

$$\therefore i_C = I_C + I_C \frac{v_{be}}{V_T}$$

i_C total current; I_C DC signal using eqn (3); $I_C \frac{v_{be}}{V_T}$ ac component (signal) using eqn (2)

ac signal current: $\boxed{i_c = I_C \frac{v_{be}}{V_T}} \rightarrow (7)$

Collector current i_c

$$i_c = I_C \cdot \frac{v_{be}}{V_T}$$

o/p / i/p → $\frac{I_C}{V_T}$ = trans conductance = g_m

o/p / i/p ⇒ trans

I/V ⇒ Conductance (inverse of resistance) (conductance is resistance)

Base current i_b

Convert i_c to i_b

$$i_b = \frac{i_c}{\beta}$$

$$i_b = \frac{I_C}{\beta} \frac{v_{be}}{V_T}$$

$$i_b = g_m \cdot \frac{v_{be}}{\beta}$$

Emitter current i_e

Convert i_c to i_e

$$i_e = i_c + i_b$$

$$i_e = i_c + i_c/\beta$$

$$i_e = i_c (1 + 1/\beta)$$

$$i_e = \left(\frac{I_C}{V_T} v_{be}\right)\left(1 + \frac{1}{\beta}\right)$$

$$i_e = g_m \cdot v_{be} \left(1 + \frac{1}{\beta}\right)$$

Resistance in Collector

$$r_c = \frac{1}{g_m}$$

also $i_c = g_m \cdot v_{be}$

Resistance in Base

$$r_b = r_\pi = \frac{\beta}{g_m}$$

also $i_b = \frac{1}{r_\pi} \cdot v_{be}$

Resistance in Emitter

$$r_e = \frac{1}{g_m\left(1 + \frac{1}{\beta}\right)}$$

also

$$i_e = \frac{1}{r_e} \cdot v_{be}$$

Base current & i/p resistance: (i_b, r_π)

$$I_B = \frac{i_G}{\beta} \rightarrow (1)$$

$$i_G = I_C + \frac{I_C}{V_T} v_{be} \rightarrow (2)$$

using (2) in (1)

$$(1) \Rightarrow i_B = \frac{I_C}{\beta} + \frac{I_C}{\beta} \cdot \frac{v_{be}}{V_T} \rightarrow (3)$$

$$i_B = I_B + i_b \rightarrow (4)$$

Compare (3) & (4) $\Rightarrow$ $i_b = \frac{I_C}{\beta} \frac{v_{be}}{V_T}$

g_m

$$\therefore \boxed{i_b = \frac{g_m}{\beta} \cdot v_{be}}$$

$$\boxed{r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m}}$$ from above eqn

Alternatively,

$$r_\pi = \frac{\beta}{I_C/V_T} \Rightarrow \boxed{r_\pi = \frac{\beta \, V_T}{I_C} \; \frac{1}{I_B}}$$

$$\boxed{r_\pi = \frac{V_T}{I_B}}$$

Emitter current & i/p resistance: (i_e, r_e)

$$i_E = \frac{i_G}{\alpha} = \frac{I_G + i_c}{\alpha}$$

$$= \frac{1}{\alpha}\left[I_C + \frac{I_C}{V_T} v_{be}\right]$$

$$i_E = I_C/\alpha + \frac{I_C}{\alpha V_T} v_{be} \rightarrow (1)$$

$\alpha I_E = I_C$; $\alpha \approx 0.99$ to $\alpha \approx 1$

Current gain factor

(or) Current amplification factor from C to E

$i_E = I_E + i_e \rightarrow (2)$

Comparing eqn (1) & (2).

$I_E = I_C/\alpha \rightarrow (3)$

$$\boxed{i_e = \frac{I_C}{\alpha V_T} v_{be}} = \frac{g_m}{\alpha} \cdot v_{be}$$

$$\boxed{r_e = \frac{v_{be}}{i_e} = \frac{\alpha V_T}{I_C} = \frac{\alpha}{g_m}} \qquad \alpha \approx 1$$

$$r_e = \frac{1}{g_m}$$

Relation b/w r_π & r_e

$$r_\pi = \frac{v_{be}}{i_b} \qquad r_e = \frac{v_{be}}{i_e}$$

$$v_{be} = r_\pi \cdot i_b = i_e \cdot r_e.$$

$$r_\pi = \frac{i_e}{i_b} r_e \Rightarrow \boxed{r_\pi = (1+\beta) r_e}$$

Voltage Gain : Gain = $^{O/P\ Vtg}/_{i/P\ Vtg}$ $\quad A_v = \frac{V_{out}}{V_{in}} = \frac{v_c}{v_{be}}$

→ The total collector voltage $v_c = V_{cc} - I_c R_c$

$\therefore v_c = V_{cc} - (I_c + i_c) R_c$

$= V_{cc} - I_c R_c - i_c R_c$

$v_c = (V_{cc} - I_c R_c) - i_c R_c$

$v_c = V_c - i_c R_c \rightarrow ①$ $\quad V_c \rightarrow$ the dc bias Vtg at Collector

$v_c = V_c - v_c \rightarrow ②$

compare eqn ① & ②

$v_c = -i_c R_c$

$v_c = -g_m v_{be} R_c$

$v_c = (-g_m R_c) v_{be}$

$\therefore$ Vtg gain $A_v = \frac{v_c}{v_{be}} = -g_m R_c$

$\therefore \boxed{A_v = \frac{I_c R_c}{V_T}}$

Problem :- ① For CE amplifier circuit, $I_C = 1mA$, $V_{CE} = 15V$, $R_C = 10K\Omega$ & $\beta = 100$. Find the Vtg gain v_c/v_{be}. If $v_{be} = 0.005 \sin \omega t$ Volt, find $v_c(t)$ & $i_B(t)$

Soln :- $A_v = \frac{I_c R_c}{V_T} = \frac{1 \times 10^{-3} \times 10 \times 10^3}{26\ mV} = -384.6$

$v_c(t) = A_v \times v_{be} = -384.6 \times 0.005 \sin \omega t$

$= -1.923 \sin \omega t$

~~$v_c = V_c - i_c R_c$~~

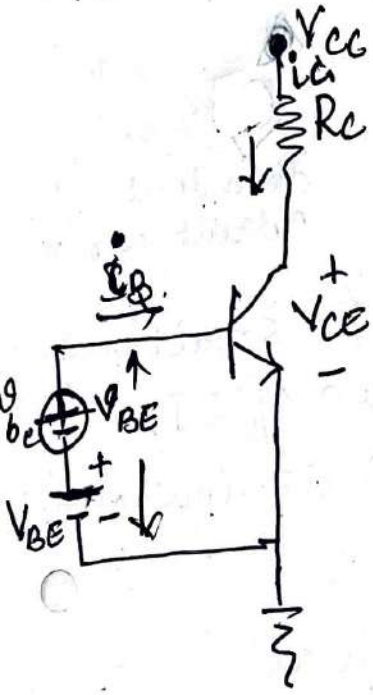
$i_B(t) = I_B + i_b$

$= \frac{I_c}{\beta} + \frac{I_c v_{be}}{\beta V_T} = \frac{1 \times 10^{-3}}{100} + \frac{1 \times 10^{-3} \times 0.005 \sin \omega t}{100 \times 0.026}$

$\boxed{i_B = 10 + 1.923 \sin \omega t\ \mu A}$

Separating the Signal and the DC Quantities:

→ Let us Consider CE Amplifier ckt. → Amplifier two components

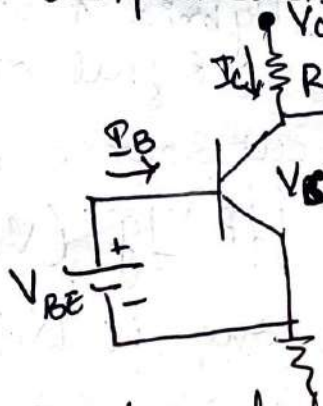


Why to separate signal?
→ to Analize amplifier ckt we need to separate ac & dc components.

(i) dc component → const over time
(ii) ac component → varies w.r.t time (signal component)

Ex:- $v_{BE} = V_{BE} + v_{be}$ (dc) (ac)

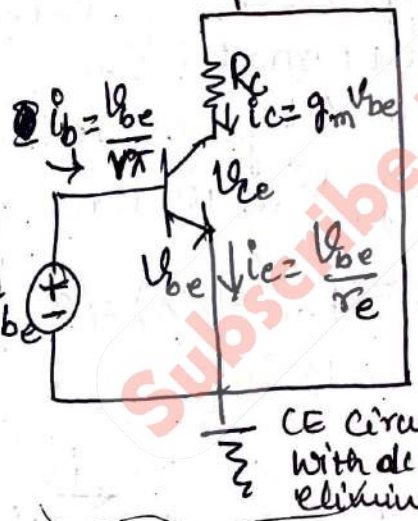
$i_C = I_C + i_c$ (dc) (ac)



CE circuit with ac source eliminated

→ DC components can be determined by making ac signal as zero.

→ AC components can be determined by eliminating dc components. V_{BE} & V_{CE} → are eliminated.
i_C, V_{CE} → determines operating point.



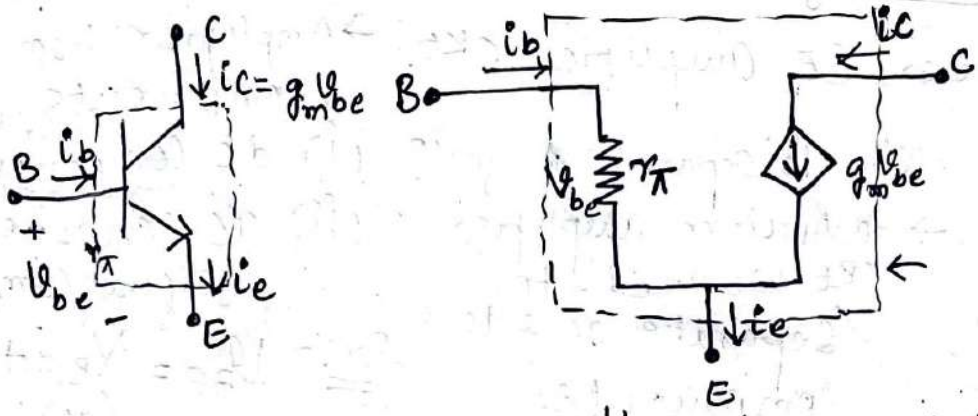
CE Circuit with dc Source eliminated.

This is not a total amplifier ckt, it is just a portion of amplifier ckt

→ by considering ac signal in amplifier
→ we will get to know all the ac signal & component are present.
→ replace dc vtgs with short Circuit (V_{BE} & V_{cc})
→ DC current source should be replaced with open Circuit.

→ Fig shows the expression for current i_b, i_e & i_c obtained for small signal V_{be} applied.

The Hybrid-π Model :



Hybrid π model for small signal operation of BJT

→ Current source (i_c) is controlled by i/p Vtg (v_{be})

→ Thats why it is known as "Voltage Controlled Current Source"

→ It is known as trans conductance Amplifier.

From model,

$i_c = g_m v_{be}$ & $i_b = v_{be}/r_\pi$

$\because i_e = i_b + i_c$

$= \frac{v_{be}}{r_\pi} + g_m v_{be}$

$= \frac{v_{be}}{r_\pi}(1 + g_m r_\pi)$

$\because r_\pi = \frac{\beta}{g_m}$

$\Rightarrow \beta = r_\pi g_m$.

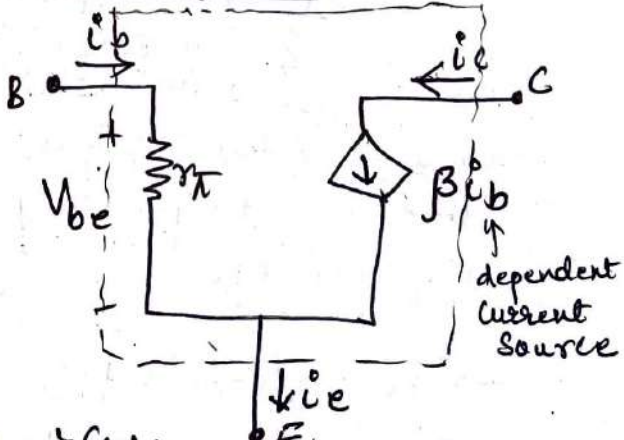
$\therefore i_e = \frac{v_{be}}{r_\pi}(1+\beta) = \frac{v_{be}}{r_\pi/(1+\beta)}$

$$\boxed{i_e = \frac{v_{be}}{r_e}}$$

→ Different equivalent Circuit model Can be Obtained by expressing Controlled Current of Source $g_m v_{be}$ in terms of i_b

$g_m v_{be} = g_m (i_b r_\pi) = (\underbrace{g_m r_\pi}_{\beta}) i_b$

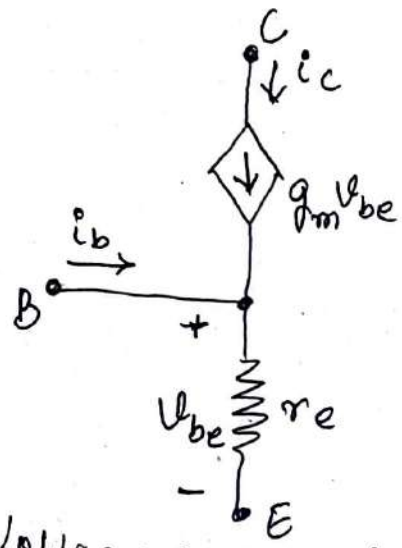
$$\boxed{g_m v_{be} = \beta i_b}$$



→ Current Source (i_c) is Controlled by i/p Current (i_b)

→ Hence it is "Current Controlled Current Source"

The T equivalent circuit Model: [BJT]



@ Voltage Controlled current source

$g_m = I_C / V_T$

$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$.

$\boxed{\alpha = g_m r_e}$

→ hybrid π model can be used to carry out small signal analysis of all transistor circuits

→ An alternative model can also be used, which is "the T model" as shown in figure.

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be}$$

$$= \frac{v_{be}}{r_e}(1 - g_m r_e)$$

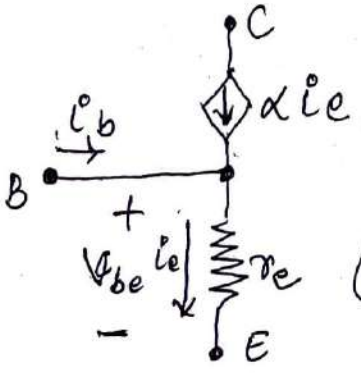
$$= \frac{v_{be}}{r_e}(1 - \alpha) \quad \because \alpha = \frac{\beta}{\beta+1}$$

$$\therefore i_b = \frac{v_{be}}{r_e}\left(1 - \frac{\beta}{\beta+1}\right) = \frac{v_{be}}{r_e}\left(\frac{\beta+1-\beta}{\beta+1}\right)$$

$$i_b = \frac{v_{be}}{(\beta+1) r_e} \Rightarrow \boxed{i_b = \frac{v_{be}}{r_\pi}} \quad \because (\beta+1) r_e = r_\pi$$

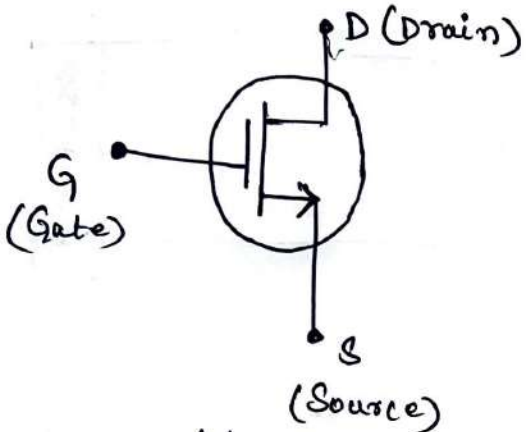
→ for current Controlled Current source.

$$g_m v_{be} = g_m (i_e r_e) = \underbrace{(g_m \cdot r_e)}_{\alpha} i_e \Rightarrow \boxed{g_m v_{be} = \alpha i_e}$$



(b) Current Controlled current source

Biasing in MOS Amplifier Circuit :-



MOSFET

Introduction:

→ MOSFET → used as an Amplifier

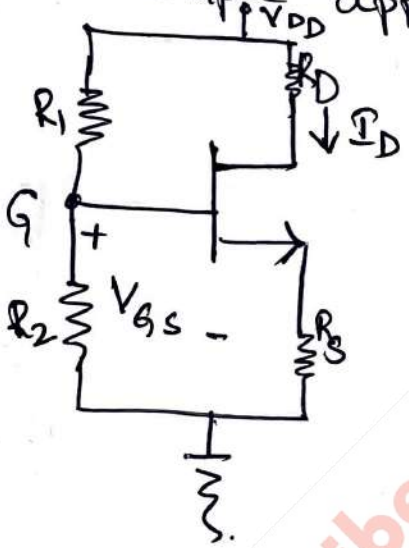
→ Biasing is important for Amplifier

→ Biasing is used to set the Q-Point.

→ Q-Point decides how MOSFET will work as Amplifier.

(1) Biasing by Fixing V_{GS} :

→ Simple approach to bias a MOSFET.



→ V_{GS} is fixed so that we can get required amount of drain current.

→ V_{GS} is increased until required amount of I_D is obtain, once I_D is sufficient then V_{GS} is maintained constant (Fixed).

→ This can be achived by using suitable V_{tg} divider circuit

→ Drain current $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$

I_D → Drain current

C_{ox} → Oxide Capacitance

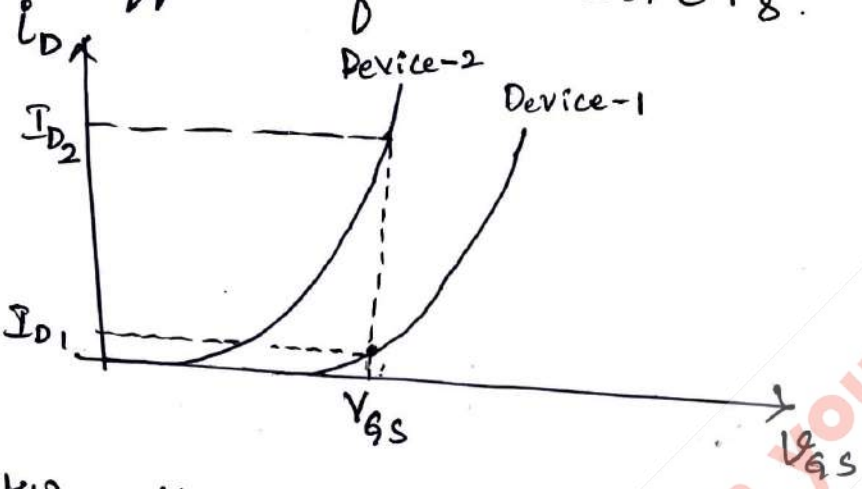
V_{GS} → V_{tg} b/w Gate & Source

V_t → threshold V_{tg}

W/L → transistor aspect ratio (width & Length)

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$$

→ If we have two MOSFETs V_t, W/L & C_{ox} will be different for two MOSFETs.

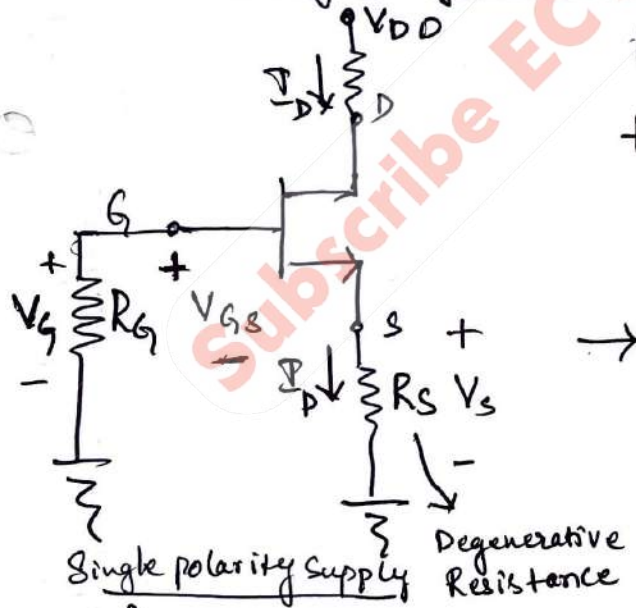


→ for two different MOSFETs if we apply same V_{GS} we will get two different Drain currents

→ two MOSFETs will not have same electrical Parameters.

→ Q-point is not stable. → This method will not be used.

(b) Biasing by Fixing V_G:-



i/p side :- KVL

$$+V_G - V_{GS} - I_D R_S = 0$$

$$V_G = V_{GS} + I_D R_S \longrightarrow (1)$$

→ V_G → constant. (Fixed)

If I_D increase due to temp change then V_{GS} should decrease.

→ if V_{GS} decreases, then i/p decreases, then drain current will also decrease.

→ R_S is the resistance that employs negative F.B. Thats why it is known as Degenerative Resistance

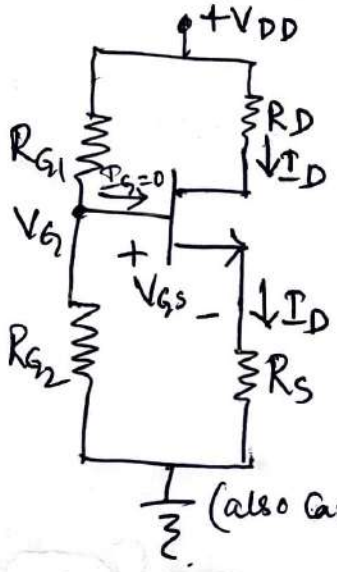
$V_G = V_{GS} + I_D R_S$ → Here I_D will be determined by values of V_G & R_S.

(i) $V_G \gg V_{GS}$ → drop V_{GS} → negligable. → I_D is maintained

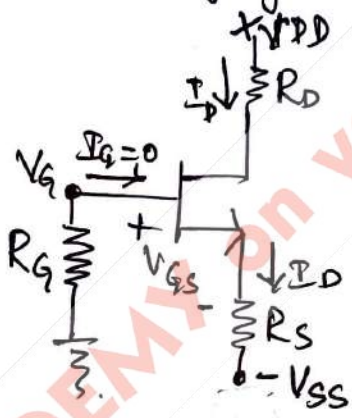
then, $\boxed{I_D = \frac{V_G}{R_S}}$

(ii) V_G not greater than V_{GS}.

then, drop V_{GS} is not negligable → then R_S provides negative feedback → which stabilizes the value of I_D.



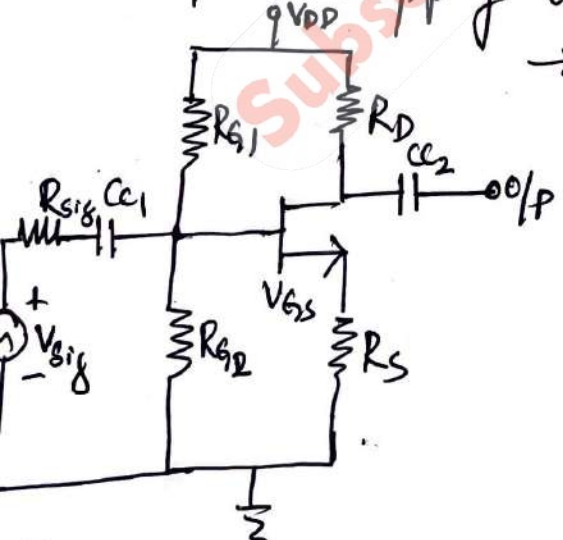
(a) using single power supply



(b) using dual power supply

@ & (b)

→ Above fig.' shows the practical implementation of biasing of MOSFET by fixing V_G using single power supply and dual power supply.



(c) Coupling of Signal source to the amplifier.

→ fig (c) shows how to connect signal source to the gate through a coupling capacitor

→ Here C_{C_1} blocks dc & allows the signal V_{sig} to gate (amplifier i/p) without affecting biasing point.

→ C_{C_2} blocks all dc & allow o/p signal to couple with other circuits.

→ C_{C_1} should be large so that it acts as short circuit to all desired frequencies

→ The value of R_D should be large enough to provide sufficient V to gain.

Problems on Small signal model.

① Find the value of g_m, r_e & r_π at the bias point if $\beta = 100$ & $I_C = 1mA$.

Soln:

$$g_m = \frac{I_C}{V_T} = \frac{1mA}{26mV} = 38.46\ mA/V.$$

$$r_e = \frac{1}{g_m\left(1+\frac{1}{\beta}\right)} = \frac{\beta}{g_m}\cdot\frac{1}{1+\beta} = \frac{100}{38.46m}\times\frac{1}{1+100}$$

$$r_e = 25.74\Omega$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{38.46m} = 2.6K\Omega$$

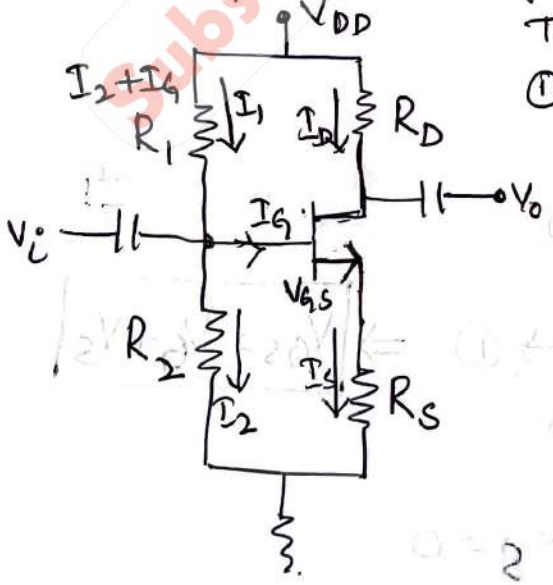
Biasing of MOSFET :

Two parameters (V_{GS}, I_D) Q-points

- Gate biasing
- Source biasing
- Voltage divider bias
- Feedback bias.

① Voltage divider bias MOSFET

(or) Biasing by Fixing V_G



Things to remember.

① R_D → o/p resistance/Drain res.
R_S → Soure biasing res.
R_1 & R_2 → Vtg divider bias res.
C_1 & C_2 → Coupling Capacitor
I_D → Dain Current

$I_D = K(V_{GS} - V_{th})^2$

K → const $K = \frac{1}{2} k_n \frac{W}{L}$ (n channel)

V_{GS} → G to S Vtg

V_{th} → threshold Vtg

> V_{th} → mosfet will turn ON
< V_{th} → mosfet will be OFF.

$I_G \to 0$ (zero) → Gate Current. (theoretically)

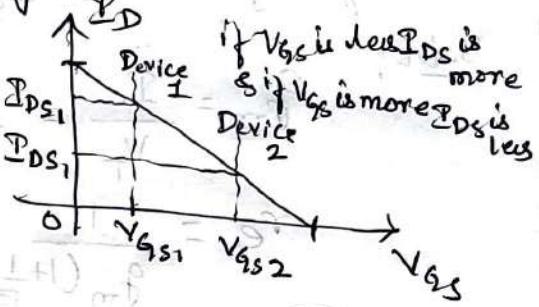
$I_D = I_G + I_S \Rightarrow I_D = I_S$ → Source Current.

I_1 & I_2 → Biasing current very very small (zero)

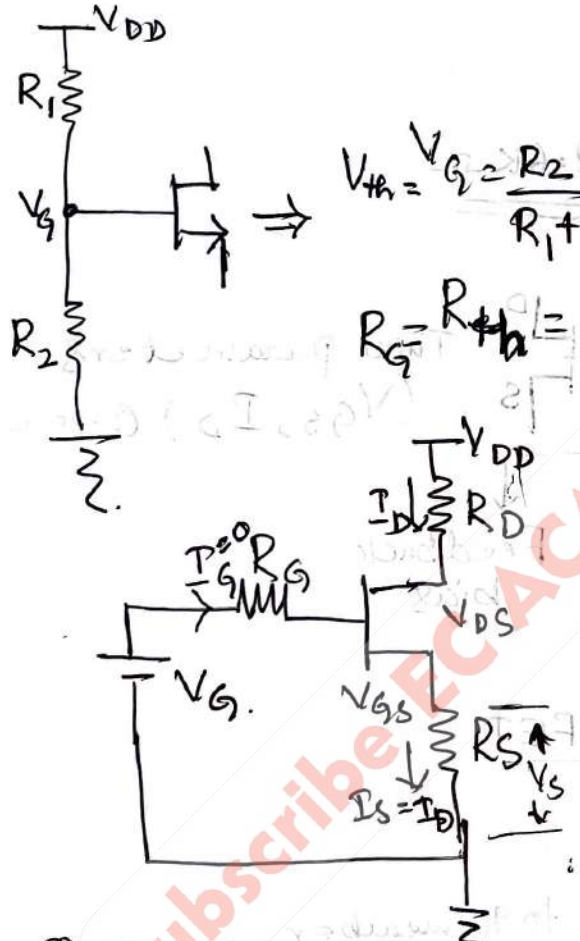
V_{DD} – power supply

V_{DS} – D to S V+g → o|p V+g

V_{GS} – i|p V+g



Step ① i|p Circuit.



$$V_{th} = V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$R_G = R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

Step ② Apply KVL to i|p

I_G ignore ∵ $I_G = 0$

$$V_G - I_G R_G - V_{GS} - I_D R_S = 0$$

$$V_G - V_{GS} - V_S = 0 \longrightarrow (1) \Rightarrow \boxed{V_{GS} = V_G + V_S}$$

Step ③ Apply KVL to o|p.

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

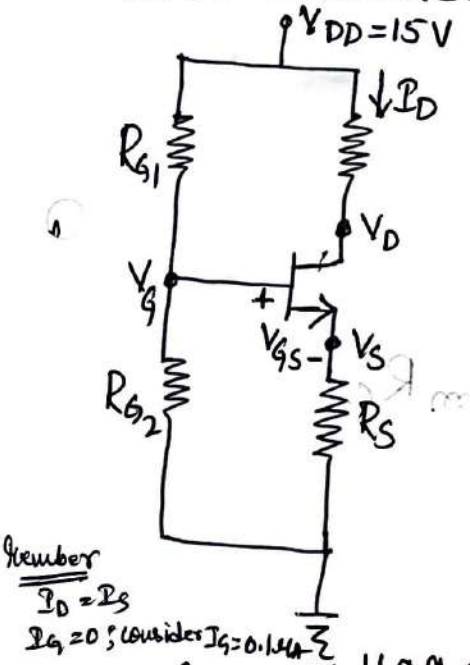
$$V_{DD} - V_{DS} - I_D (R_D + R_S) = 0$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Problems :-

(1) Design the circuit shown in figure to establish $I_D = 0.5mA$. MOSFET Parameters are $V_t = 1V$, $K_n' W/L = 1mA/V^2$ & $\lambda = 0$



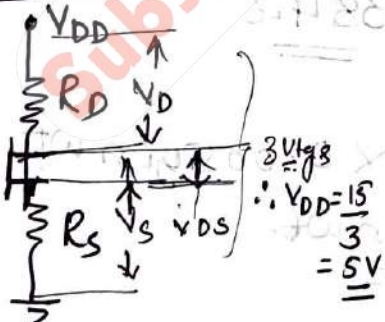
Remember
$I_D = I_S$
$I_G = 0$; consider $I_G = 0.1\mu A$

Step ①:- find Voltages.

V_{DS} V_S V_{DD} V_G V_{GS}.

V_{DD} ↓ 15V (given).

V_S ↓ to find use thumb rule



$V_S = 5V$.

$V_{DS} = V_D + V_S = 5V + 5V$

$V_{DS} = 10V$

$V_{GS} =$

$I_D = K(V_{GS} - V_{th})^2$ $\quad K = \frac{1}{2} K_n' W/L$

$K = \frac{1}{2} \times 1mA$.

$0.5mA = \frac{1}{2} \times 1m (V_{GS} - 1)^2$.

$V_{GS} = 2V$.

$V_G - V_{GS} - V_S = 0$.

$V_G = V_{GS} + V_S = 2 + 5 \Rightarrow V_G = 7V$

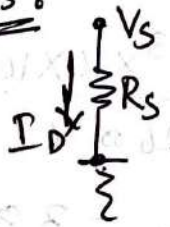
Step ②:- find resistance.

R_D:-

$R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{15 - 10}{0.5mA}$

$R_D = 10K\Omega$

R_S:-



$R_S = \frac{V_S - 0}{I_D} = \frac{5 - 0}{0.5m}$

$R_S = 10K\Omega$.

R_{G1} & R_{G2} :-

$R_{G1} = \frac{V_{DD} - V_G}{I_1}$

$I_1 = I_2 + I_G$

$I_1 = 1.14\mu A$

$I_2 = 10 I_G$

$I_2 = 10 \times 0.1\mu$

$I_2 = 1\mu A$

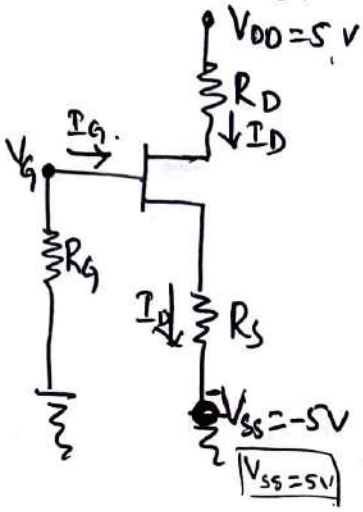
$R_{G1} = \frac{15 - 7}{1.14\mu A}$

$R_{G1} = 8M\Omega$

$R_{G2} = \frac{V_G - 0}{I_2} = \frac{7}{1\mu} = 7M\Omega$

(9) (i) Design the CKt as shown where $I_D = 0.5mA$, $V_t = 1V$, $K_n' W/L = 1mA/V^2$ and $\lambda = 0$

(ii) Use Standard Resistor Values & give the resulting values of I_D, V_D, & V_S.

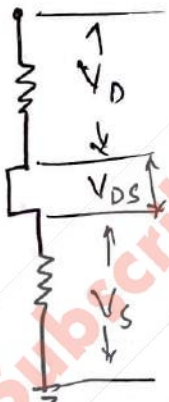


Step ① :- find voltages.

V_{DS}, V_S, V_{DD}, V_G, V_{GS}.

V_{DD} ↓ 5V.

V_{DS}, V_S ↓ Thumbrule.



$S/3 = 1.66$

$V_S = 1.66V$

$V_{DS} = V_D + V_S = 3.32V$

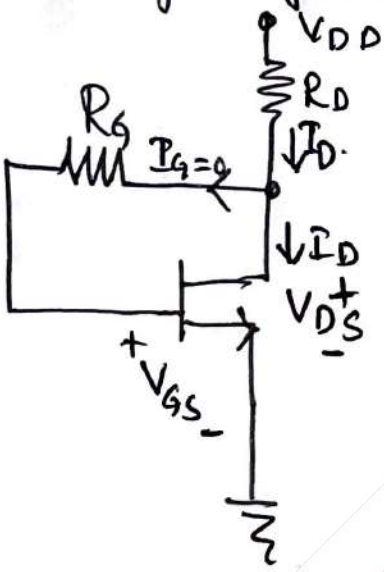
(3) For designed circuit in example (1) when MOSFET is replaced with another having $V_t = 1.5V$, what will be the new value of I_D.

$$I_D = \frac{1}{2} \times K_n' (W/L) (V_{GS} - V_{th})$$

$$I_D = 1/2 \times 1 \times 10^{-3} (2 - 1.5)^2$$

$$I_D = 0.125 mA$$

Biasing by Drain to gate Feedback Resistor:



i/p side:-

$V_{DD} - I_D R_D - I_G R_G - V_{GS} = 0$ (I_G ignore $\because I_G = 0$)

$$V_{GS} = V_{DD} - I_D R_D \rightarrow (1)$$

o/p side:-

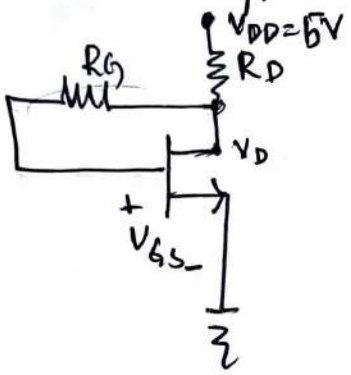
$V_{DD} - I_D R_D - V_{DS} = 0$.

$I_D R_D = V_{DD} - V_{DS}$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} \rightarrow (2).$$

$$V_{DS} = V_{DD} - I_D R_D.$$

① Design the circuit as shown where $I_D = 0.5mA$, $V_t = 1V$, $K_n' W/L = 1mA/V^2$



① find Vtages:-

$V_{DD} = 5V$ V_D V_{DS} V_G V_{GS}

$V_D = V_G = V_{GS}$

$I_D = K(V_{GS} - V_t)^2$

$\because K = \frac{1}{2} K_n' W/L \Rightarrow I_D = \frac{1}{2} K_n' W/L (V_{GS} - V_t)^2$

$0.5 = \frac{1}{2} \times m (V_{GS} - 1)^2$

$V_D = V_G = \boxed{V_{GS} = 2V}$

② Find Resistance

ⓐ $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5-2}{0.5m} \Rightarrow \boxed{R_D = 6K\Omega}$

ⓑ $R_G = \frac{V_G}{I_G} = \frac{2}{0.1\mu} \Rightarrow \boxed{R_G = 20M\Omega}$

MOSFET Small Signal operating Model

aim is to find ac currents ac Vtg

Vtages

V_{GS} → DC source

v_{gs} → ac source

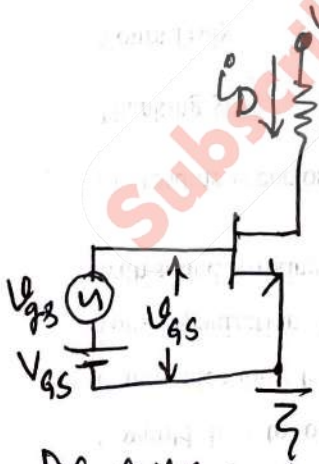
v_{GS} → Total source.

Current

I_D → DC current

i_d → ac current

i_D → total current



Total Vtg = ac + dc

$v_{GS} = v_{gs} + V_{GS} \rightarrow ①$

Total curr = ac + dc

$i_D = i_d + I_D \rightarrow ②$

DC current,

$I_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_t)^2 \rightarrow ③$

Total current

$i_d = \frac{1}{2} K_n \frac{W}{L} [(\overset{a}{V_{GS}} + \overset{b}{v_{gs}}) - \overset{c}{V_t}]^2 \rightarrow ④$

apply $(a+b-c)^2$ formula for eqn (4)

$= a^2+b^2+c^2+2ab-2bc-2ca$

(4) $\Rightarrow i_D = \frac{1}{2} K_n \frac{W}{L} \left[V_{GS}^2 + v_{gs}^2 + V_t^2 + 2V_{GS} \cdot v_{gs} - 2 v_{gs} V_t - 2 V_t V_{GS} \right]$

Find AC current :- (find terms with v_{gs} & V_t present)

Considering only ac components.

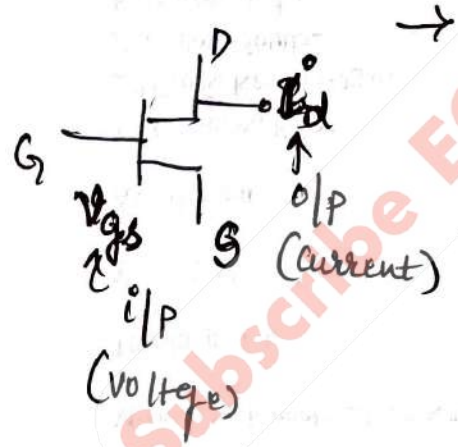
$$i_d = \frac{1}{2} K_n \frac{W}{L} (2 V_{GS} \cdot v_{gs} - 2 v_{gs} V_t)$$

$$\boxed{i_d = \frac{1}{2} K_n \frac{W}{L} \left[2 v_{gs} (V_{GS} - V_t) \right]}$$

$$\boxed{i_d = K_n \frac{W}{L} (v_{gs} (V_{GS} - V_t)} \quad \rightarrow (5)$$

Transconductance g_m :-

→ Voltage Controlled current source.



transistor → $\frac{i_c}{i_b} = \beta$ (current gain)

$I_G = 0$

i/p → v_{gs}

o/p → i_d

$\frac{\text{o/p}}{\text{i/p}} = \frac{i_d}{v_{gs}}$

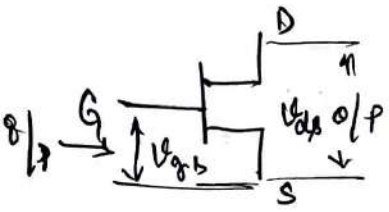
↓ trance ↓ Conductance (g_m)

$\therefore g_m = \frac{I_D}{V_{GS}}$ $\quad g_m = \frac{i_d}{v_{gs}}$

from eqn (5) $\frac{i_d}{v_{gs}} = \boxed{K_n \frac{W}{L} (V_{GS} - V_t) = g_m}$

Voltage gain

gain = o/p / i/p Voltage gain = o/p V+g / i/p V+g

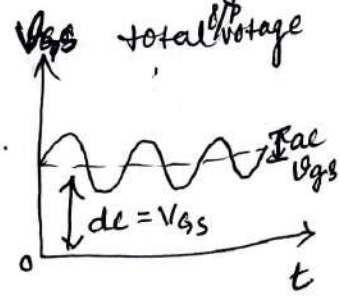


$$A_V = \frac{v_{ds}}{v_{gs}} = \frac{i_d \cdot R_D}{v_{gs}}$$ ($\frac{i_d}{v_{gs}} = g_m$)

$$\boxed{A_V = g_m \cdot R_D}$$

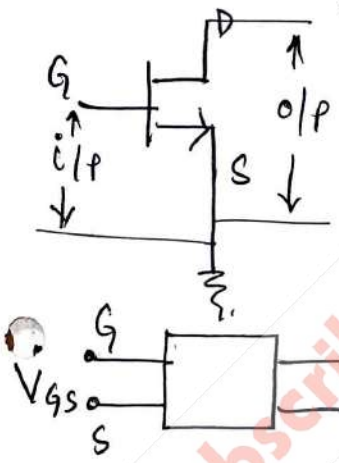
$$\frac{v_{ds}}{v_{gs}} = g_m R_D$$

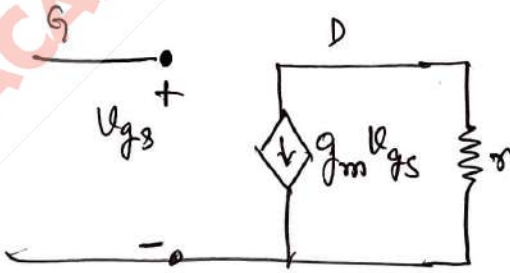
$$v_{ds} = g_m R_D V_{gs}.$$



Small Signal equivalent Model

Source configuration (Source is common)

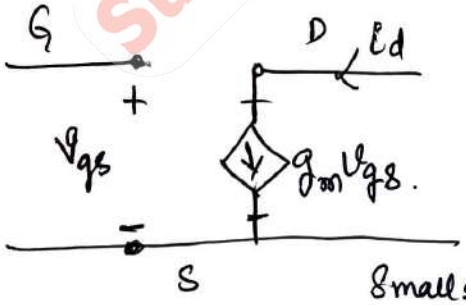




r_o internal resistance $r_o = \frac{V_o}{I_D}$.

Small signal model with r_o

$$A_V = g_m \cdot (R_D || r_o)$$



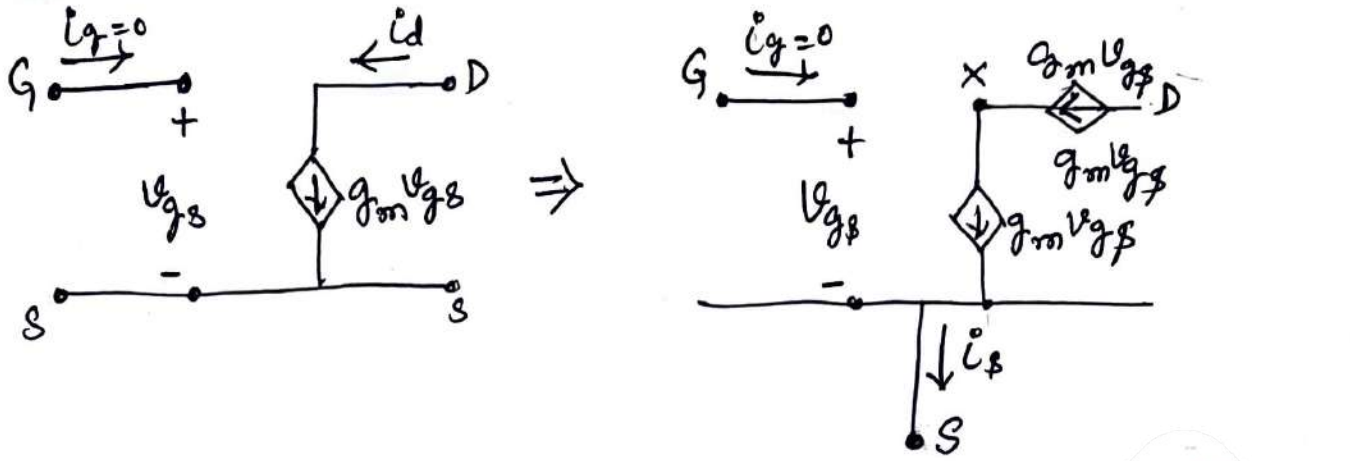
Small signal model without r_o

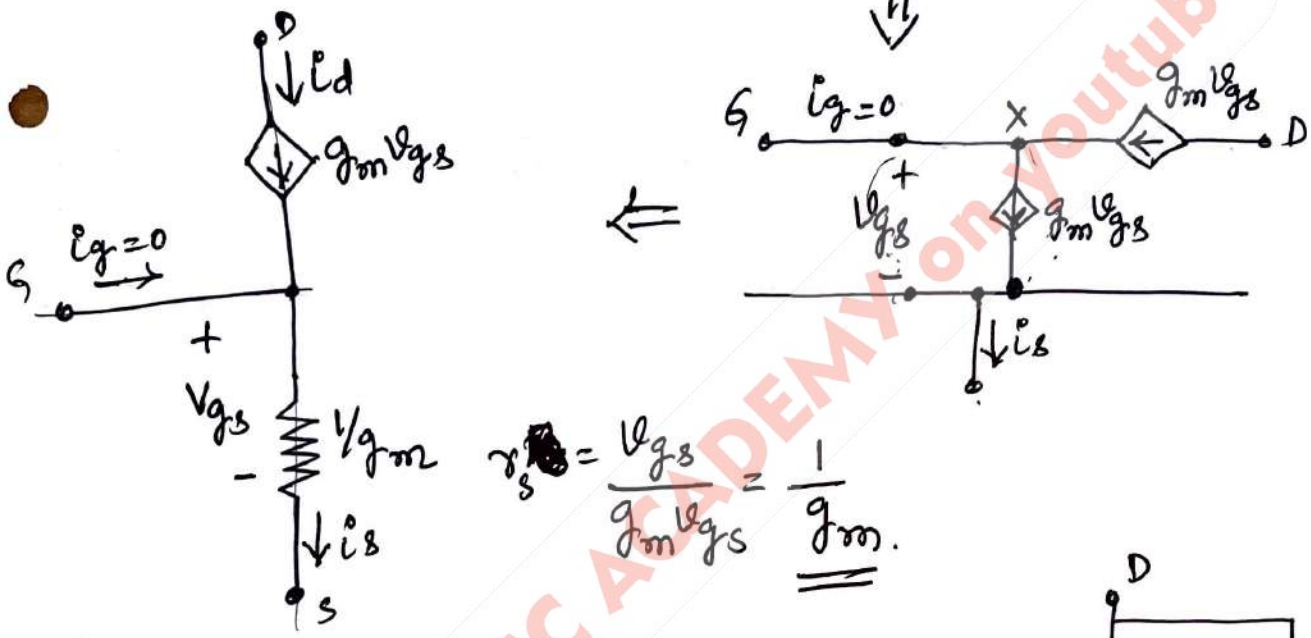
$$i_d = g_m \cdot v_{gs}.$$

$$\because g_m = \frac{i_d}{V_{gs}}.$$

$$A_V = g_m \cdot R_D$$

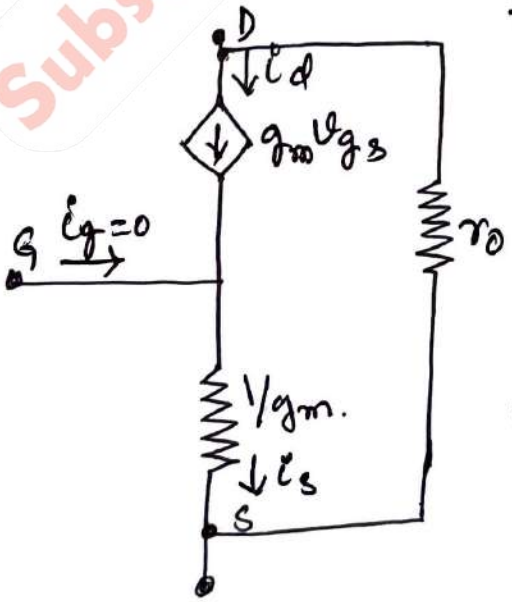
T-equivalent Circuit Model (MOSFET) :-



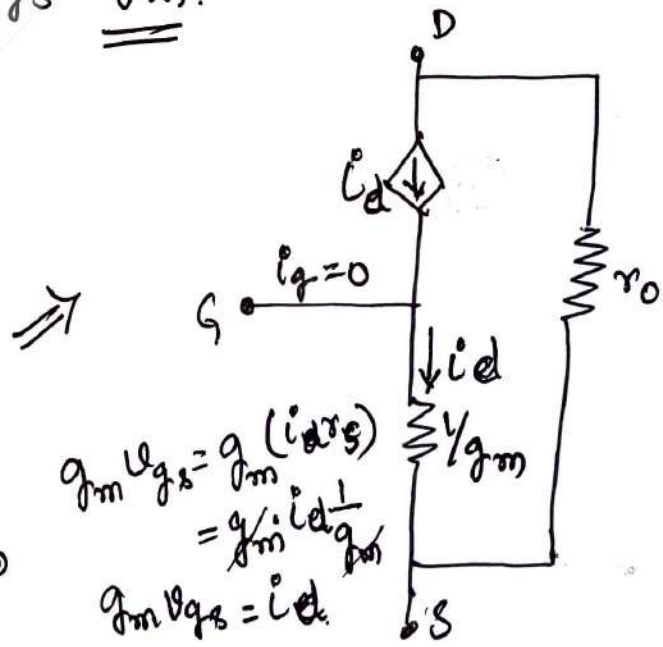


$$r_s = \frac{v_{gs}}{g_m v_{gs}} = \frac{1}{g_m}.$$

T-equivalent circuit model for MOSFET



Voltage Controlled Current Source



$g_m v_{gs} = g_m (i_d r_s)$

$= g_m i_d \frac{1}{g_m}$

$g_m v_{gs} = i_d$

Alternative representation T-model with r_o:

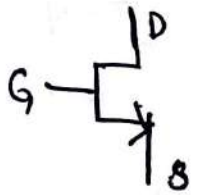
AEC

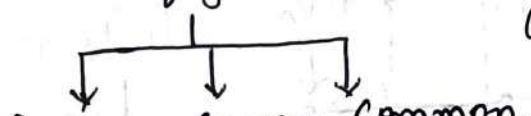
21EC34

Module-2

Module-2

MOSFET Amplifier Configuration

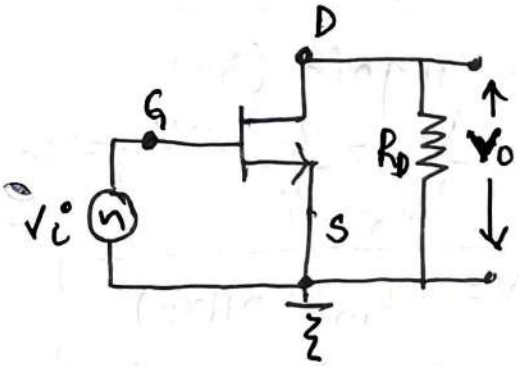




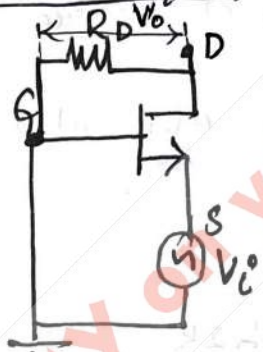
Preferably G → i/p, D → o/p

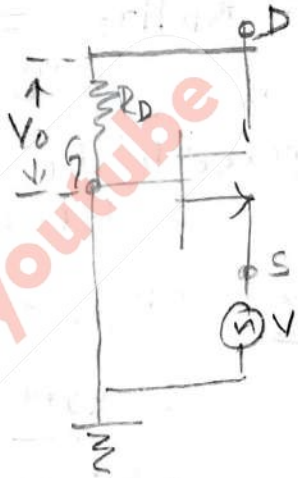
Conf.	G	S	D
CS	i/p	GND	o/p
CG	GND	i/p	o/p
CD	i/p	o/p	GND

1) Common source

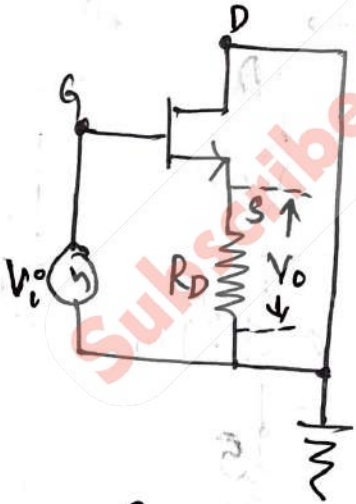


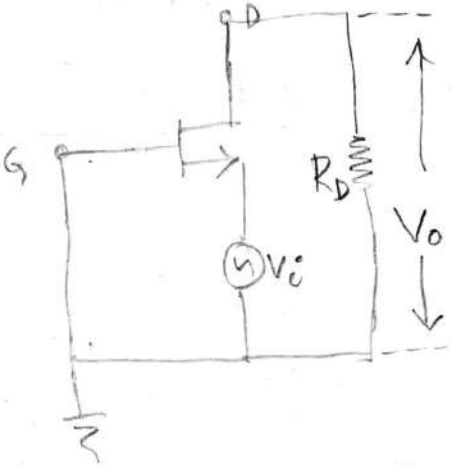
2) Common Gate





3) Common drain.

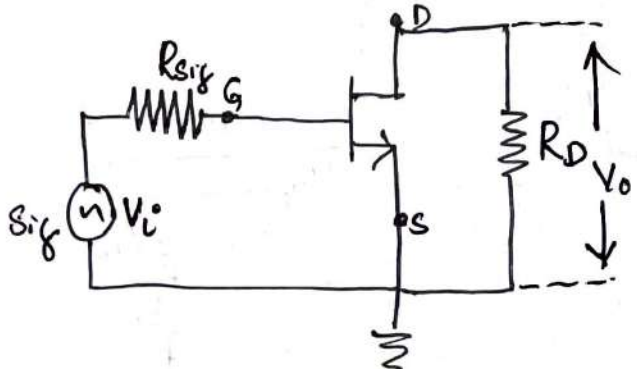




Hybrid π → no resistance at Source
T-model → resistance at Source

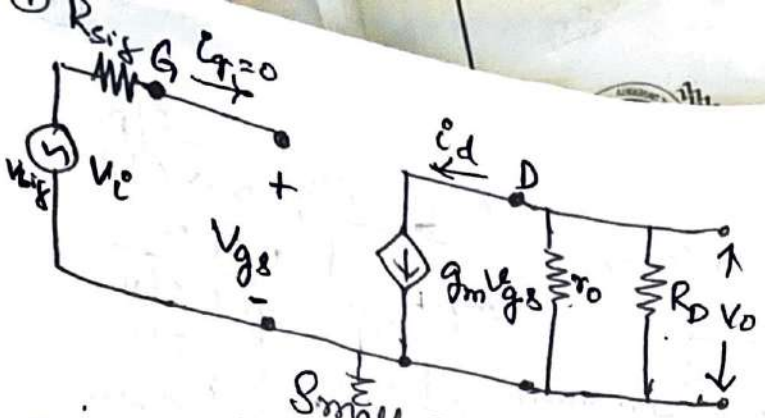
@

I. Common Source Configuration: [without RS resistor]



Remember :-

1. Convert to small signal model
2. Find R_{in}, R_o, A_v. → $\frac{V_o}{V_i}$
3. V_o & V_i



Small signal eqv model

② (a) $R_{in} = R_{sig} = \infty$ ∵ $i_g = 0$

$R = \frac{v}{i} = \frac{v}{0}$

$R = \infty$

→ Any configuration with Gate as i/p

$R_{in} = R_{sig} = \infty$

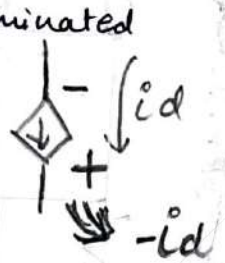
(b) $R_o = R_D \| r_o \Rightarrow$ $R_o = R_D$

→ here r_o will be very higher value compared to R_D.

→ hence r_o will be eliminated

Ex:- $2K \| 2M$

$\frac{2K \times 2M}{2K + 2M} \simeq 2K$



Current moving from -ve to +ve is -ve

③ $A_v = \frac{V_o}{V_i} = \frac{-i_d (R_D \| r_o)}{v_{gs}}$

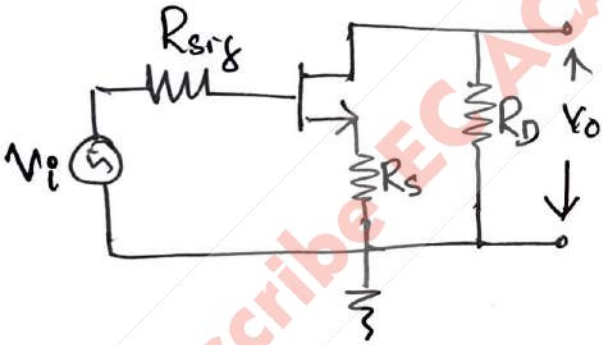
$A_v = -g_m (R_D \| r_o)$

④ overall gain (G_v)

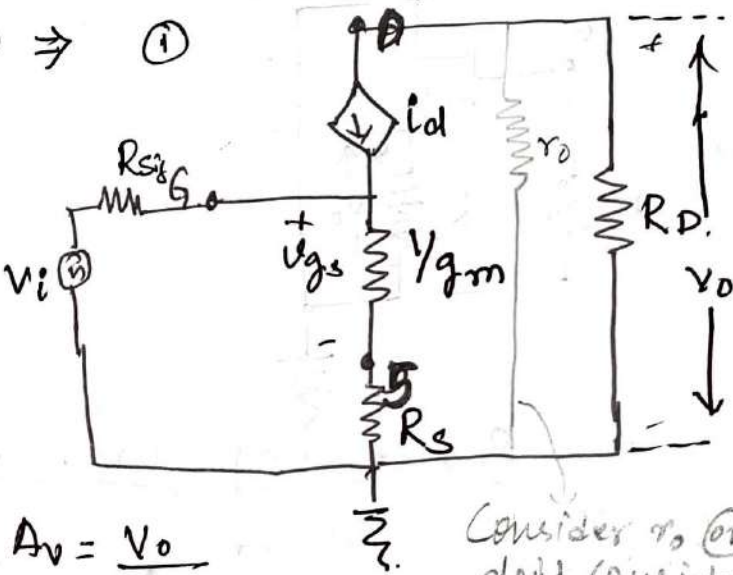
$G_v = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i}$ ∵ $V_{sig} = V_i$

$G_v = -g_m (R_D \| r_o)$

I. (b) Common Source Configuration : [with RS]



⇒ ①



Consider r_o (or) don't consider

② (a) $R_{in} = R_{sig} = \infty$

(b) $R_o = R_D$

③ $A_v = \frac{V_o}{V_i}$

$A_v = \frac{-i_d \cdot R_D}{v_{gs}(1 + g_m R_s)}$

$A_v = -g_m \cdot \frac{R_D}{(1 + g_m R_s)}$

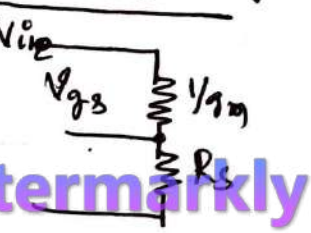
V_i Calculation :-

$v_{gs} = \frac{1/g_m}{1/g_m + R_s} V_{in}$

X by Nr. & Dr. by g_m

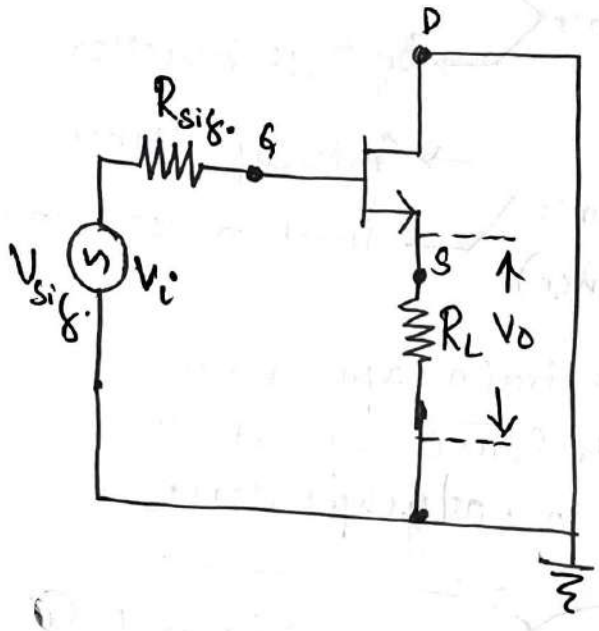
$v_{gs} = \frac{1}{1 + g_m R_s} \cdot V_{in} \Rightarrow V_{in} = v_{gs}(1 + g_m R_s)$

V_i calculation :

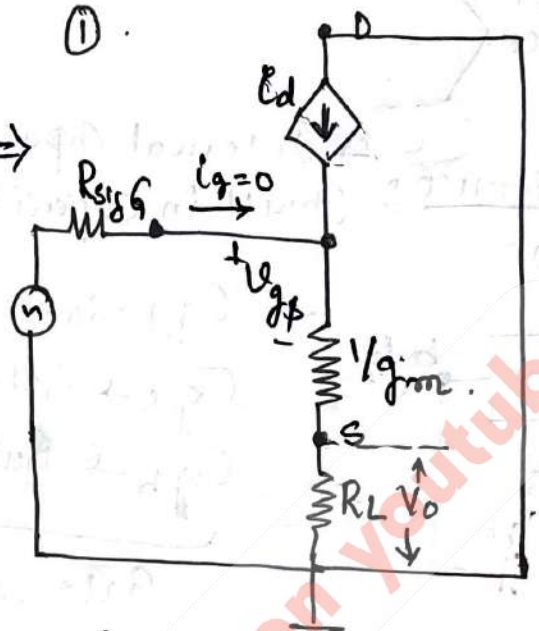


II Common drain Amplifier : (Source follower) (3)

→ ∵ o/p is obtained across the Source terminal



(1)



Small signal Model.

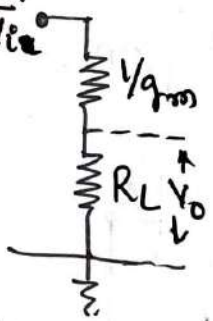
(2) $R_{in} = R_{sig} = \infty$

(3) $A_v = \frac{V_o}{V_i} =$

to find R_o make $V_{in} = 0$

$R_o = \frac{1}{g_m} \| R_L$

to find V_o :-



$V_o = \frac{R_L}{\frac{1}{g_m}+R_L} V_i$

R_L is very much large

$\therefore R_o \cong \frac{1}{g_m}$

$\therefore A_v = \frac{R_L}{1/g_m + R_L} \cdot \frac{V_i}{V_i}$

$$A_v = \frac{R_L}{1/g_m + R_L}$$

(4) overall gain (G_v)

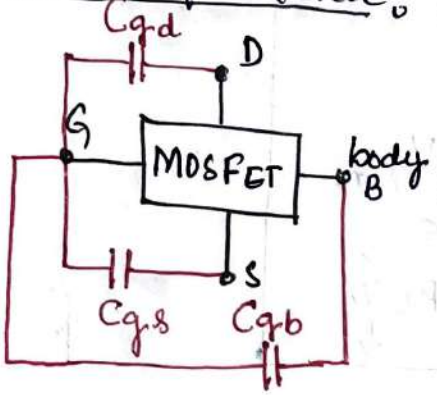
$G_v = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i}$ $\because V_{sig} = V_i$

$$\therefore G_v = \frac{R_L}{1/g_m + R_L}$$

MOSFET Internal Capacitance :-

MOSFET Capacitance
- → External Capacitance
  - → Coupling Capacitor
  - → by Pass Capacitor
- → Internal Capacitance (built-in capacitance)
  - → Gate Capacitance
  - → Junction Capacitance

Gate capacitance :



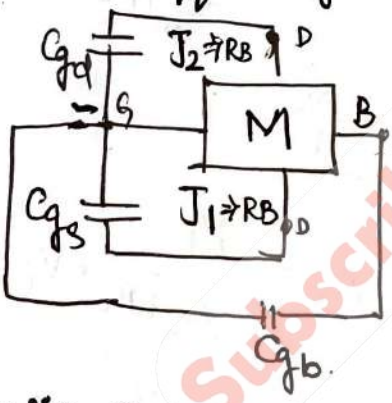
→ C_{gd} → Gate to drain Capacitance
C_{gs} → Gate to Source Capacitance
C_{gb} → Gate to body Capacitance

Gate Capacitance (or) Oxide Capacitance

→ $C_g = C_{ox} \cdot WL$ $\quad C_{ox} = \frac{E_{ox}}{t_{ox}}$

Any Storage device Can be directly proportional to width & Length.

(i) Cutoff region :-



$\because C_{gd} = 0$
& $C_{gs} = 0$
$C_{gb} = C_{ox} W \cdot L$.

(ii) Saturation :-

$C_{gb} = 0$ ∵ channel depth is max at Souce & zero at drain.

60% of Capacitance $C_{gs} = \frac{2}{3} C_{ox} WL$

$C_{gd} = 0$ → Channel dept is max at source and zero at drain

(iii) Active region :-

(it will be oppoite of Cut off region)

$C_{gb} = 0$

$C_{gd} = 1/2\, C_{ox} WL$ } equally distributed

$C_{gs} = 1/2\, C_{ox} WL$

Junction Capacitance:-

Two junctions

(i) Jun b/w drain-substrate (C_{db})

(ii) Jun b/w Source-substrate (C_{sb})

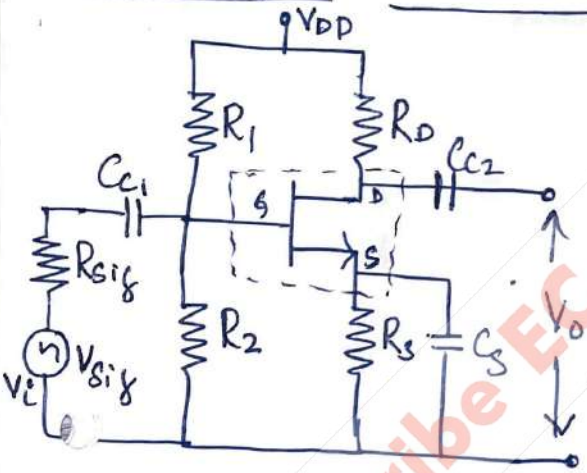
$$C_{db} = \frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{V_0}}} \quad \& \quad C_{sb} = \frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{V_0}}}$$

C_{db0} → Capacitance at $V_{DB}=0$

C_{sb0} → Capacitance at $V_{SB}=0$.

V_0 → junction built in potential (0.6 to 0.8 V)

Low Frq Response of MOSFET Amplifier:



R_D → Drain resistor (o/p)

R_S → Source resistor

R_1 & R_2 → Vtg divider bias Resistors

C_{c_1} & C_{c_2} → Coupling Capacitor

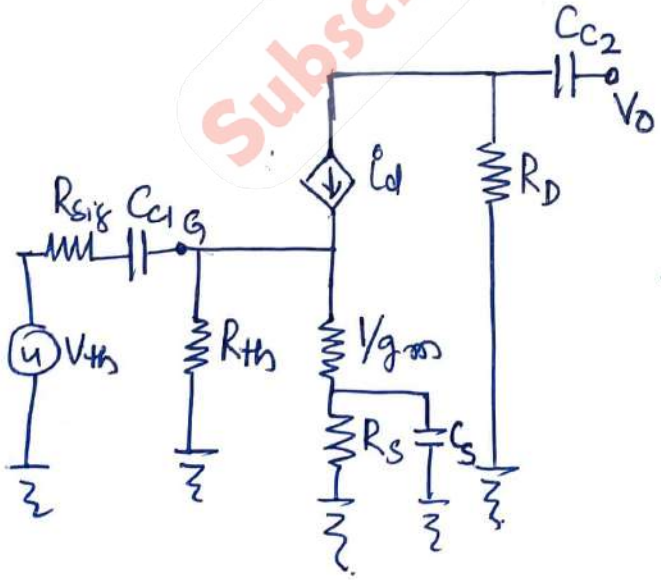
C_S → bypass capacitor.

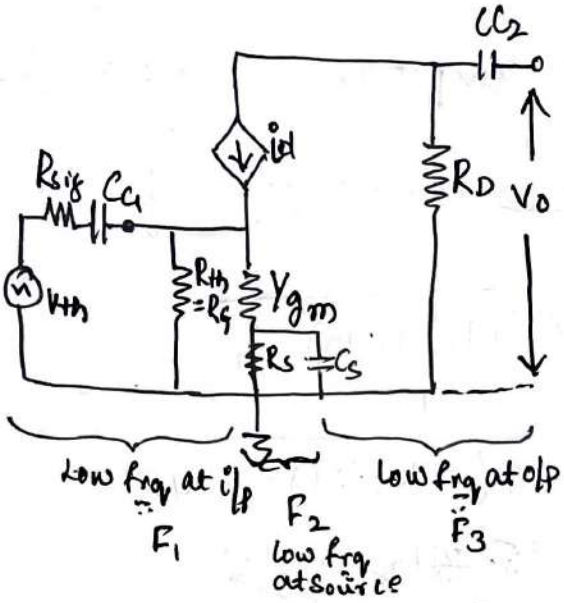
→ we need to write dc equivalent circuit (small signal model)

→ to do this (i) DC signal should be grounded

(ii) short circuit capacitors.

→ since we are discussing about small signal model we ~~not~~ require Coupling capacitors hence we will not short circuit capacitors



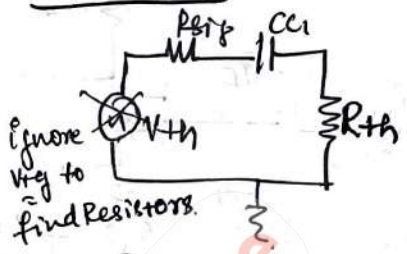


$$F = \frac{1}{2\pi RC} \Rightarrow \omega = 2\pi F = \frac{1}{RC} \qquad \boxed{\omega = \frac{1}{RC}}$$

Case (i) F_1, ω_1

$$F_1 = \frac{1}{2\pi R_{eq} C_{eq}}$$

i/p side

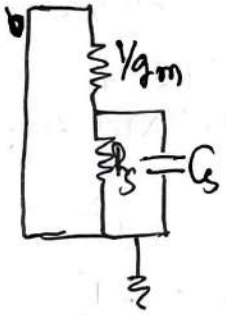


$R_{eq} = R_{sig} + R_{th}$.

$C_{eq} = C_{C_1}$

$$\therefore F_1 = \frac{1}{2\pi (R_{sig}+R_{th}) C_{C_1}} \qquad \omega_1 = \frac{1}{(R_{sig}+R_{th}) C_{C_1}}$$

Case (ii) F_2, ω_2



$$F_2 = \frac{1}{2\pi R_{eq} C_{eq}}$$

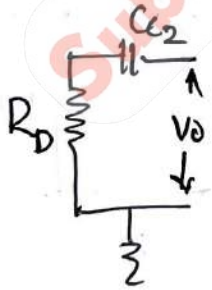
$R_{eq} = 1/g_m \,||\, R_s$ $\quad \because R_s >>> \frac{1}{g_m}$

$C_{eq} = C_s$ $\quad \therefore R_{eq} = 1/g_m$

$$F_2 = \frac{1}{2\pi (1/g_m \,||\, R_s) C_s} \Rightarrow F_2 = \frac{1}{2\pi (g_m) C_s}$$

$$\omega_2 = \frac{1}{R_{eq} \cdot C_{eq}} = \frac{1}{(1/g_m \,||\, R_s) C_s} \Rightarrow \omega_2 = \frac{1}{1/g_m C_s}.$$

Case (iii) F_3 ω_3

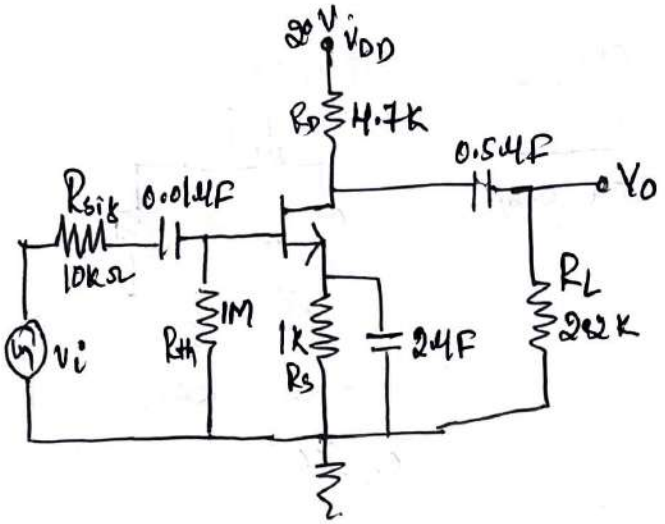


$$F_3 = \frac{1}{2\pi R_D C_{C_2}} \qquad \omega_3 = \frac{1}{R_D C_{C_2}}$$

For low frq $F_L = \max(F_1, F_2, F_3)$

Problem :-

① Find lower Cutoff frq for MOSFET amplifier $K = 0.4\ mA/V^2$ & $V_t = 1V$, $g_m = 2m$



Case (i) input ckt to find F_1

$$F_1 = \frac{1}{2\pi (R_{sig} + R_{th}) C_{C_1}}$$

$$F_1 = \frac{1}{2\pi (10K + 1M)\, 0.01\mu F}$$

$$F_1 = 15.75\ Hz$$

Case (ii) Source ckt to find F_2

$$F_2 = \frac{1}{2\pi (1/g_m \,||\, R_s) C_s}$$

find $g_m = \frac{i_d}{V_{GS}}$

To find i_d use thumb rule

$$i_d = \frac{V_{DD}}{3} = \frac{20/3}{4.7K} = \frac{20/3}{4.7K}$$

$$i_d = 1.418 \times 10^{-3} A$$

$$i_d = K (V_{GS} - V_T)^2$$

$$1.418m = 0.4m (V_{GS} - 1)^2$$

$$3.54 = (V_{GS} - 1)^2 \Rightarrow 1.88 = V_{GS} - 1$$

$$V_{GS} = 2.88$$

$g_m = 2m$

$$F_2 = \frac{1}{2\pi (1/2m \,||\, 1K) 2\mu}$$

$\frac{1}{g_m} = \frac{1}{0.5m} = 2K$

$$F_2 = \frac{1}{2\pi (2K \,||\, 1K) 2\mu}$$

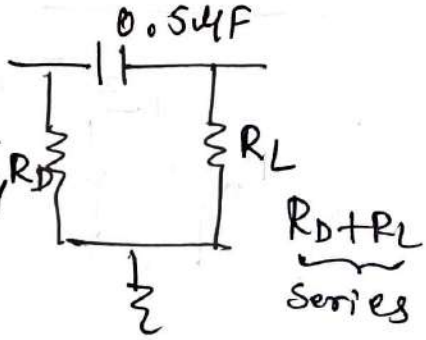
$0.667K$

$$F_2 = 119.3\ Hz$$

Case (iii) Output Circuit to find F_3

$$F_3 = \frac{1}{2\pi (R_D + R_L) C_2} = \frac{1}{2\pi (4.7K + 2.2K) 0.5\mu}$$

$$F_3 = 46.13\ Hz$$



$$F_L = \max (F_1, F_2, F_3)$$

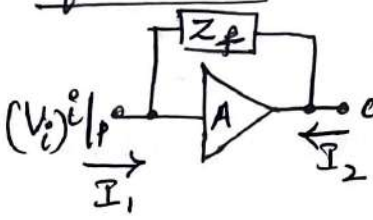
$119.3\ Hz$

Low frq $F_L =$ _____

→ This shows that if Hg divider bias ckt is used then frq should be more than 119.3 Hz Only then it will act

High freq response of MOSFET:

Miller Theorem:-



$Z_f \rightarrow$ impedence.

i/p CKt	o/p CKt

(1) o/p CKt

$$I_2 = \frac{V_o - V_i}{Z_f} \Rightarrow I_2 = \frac{V_o + V_o/A}{Z_f}$$

$$V_i = \frac{V_o}{A} \qquad I_2 = \frac{V_o(1+1/A)}{Z_f}$$

$$Z_{mo} = \frac{V_o}{I_2} = \frac{V_o}{\frac{V_o(1+1/A)}{Z_f}}$$

$$\boxed{Z_{mo} = \frac{Z_f}{(1+1/A)}}$$

$$\boxed{X_{Co} = \frac{X_{Cf}}{(1+1/A)}}$$

$$\frac{1}{\omega C_{mo}} = \frac{1}{\omega C_f (1+1/A)}$$

$$C_{mo} = C_f\left(1+\frac{1}{A}\right)$$

(2) i/p CKt

$$I_1 = \frac{V_i - V_o}{Z_f}$$

$\because V_o = -AV_i$

$$I_1 = \frac{V_i + AV_i}{Z_f}$$

$$I_1 = \frac{V_i(1+A)}{Z_f}$$

$\because Z_{mi}$ + miller's i/p.

$$\Rightarrow Z_{mi} = \frac{V_i}{I_1} = \frac{V_i}{\frac{V_i(1+A)}{Z_f}}$$

$$\boxed{Z_{mi} = \frac{Z_f}{(1+A)}}$$

$Z = X_C$ ↓ Reactance

$$\therefore \boxed{X_{Ci} = \frac{X_{Cf}}{(1+A)}}$$

$$X_C = \frac{1}{\omega C}$$

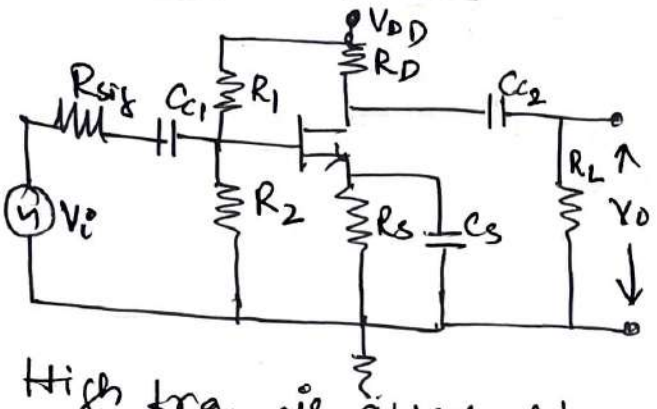
$$\frac{1}{\omega C_{mi}} = \frac{1}{\omega C_f (1+A)}$$

$$\boxed{C_{mi} = C_f(1+A)}$$

* [These derivation not in VTU Syllabus only for understanding] *

→ If any capacitor is connected as feedback b/w i/p & o/p, the feedback capacitance can be isolated in two parts as i/p part & o/p part. [C_i & C_o]

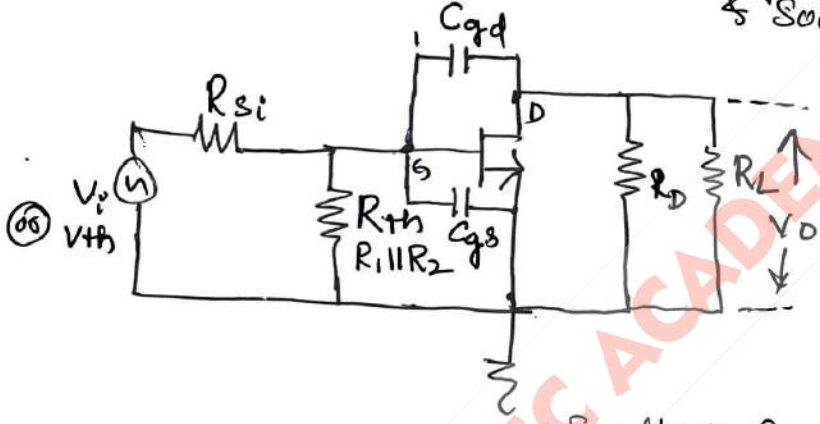
High Freq response :-



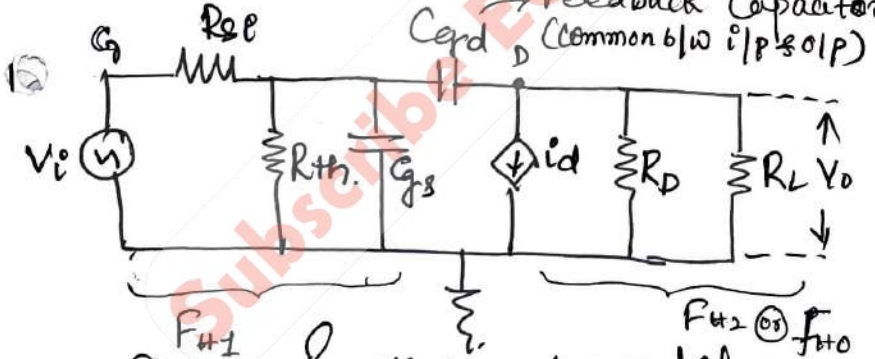
$R_D \rightarrow$
$R_s \rightarrow$
R_1 & $R_2 \rightarrow$
$R_L \rightarrow$
C_{c1} & $C_{c2} \rightarrow$
$C_s \rightarrow$
$V_{DD} \rightarrow$

High freq is affected by internal capacitance (or) inbuilt capacitance.

Small signal model → (1) DC source ⇒ GND.
(2) coupling & bypass capacitor & source resistance ⇒ SHORT CKT.



→ Feedback Capacitor (common b/w i/p & o/p)

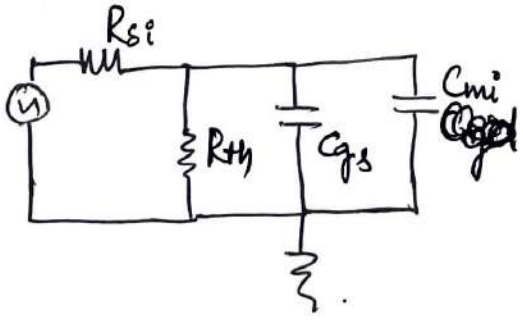


or F_{Hi} Small signal model.

$$\omega_{Hi} = \frac{1}{(R_{si} \| R_{th}) C_{gs} + C_{mi}}$$

(i) Case Input CKT F_{Hi}

$$F_{Hi} = \frac{1}{2\pi R_{eq} C_{eq}}$$



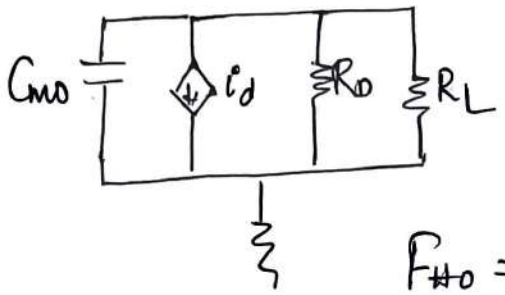
$$C_{mi} = C_{gd}(1+A)$$

$$C_{eq} = C_{gs} + C_{mi}$$

$$R_{eq} = R_{si} \| R_{th}$$

$$\therefore F_{Hi} = \frac{1}{2\pi (R_{si} \| R_{th}) C_{gs} + C_{mi}}$$

(ii) Case o/p ckt F_{Ho} $f_{Ho} = \frac{1}{2\pi R_{eq} C_{eq}}$ $C_{mo} = C_{gd}(1+1/A)$



$C_{eq} = C_{mo}$

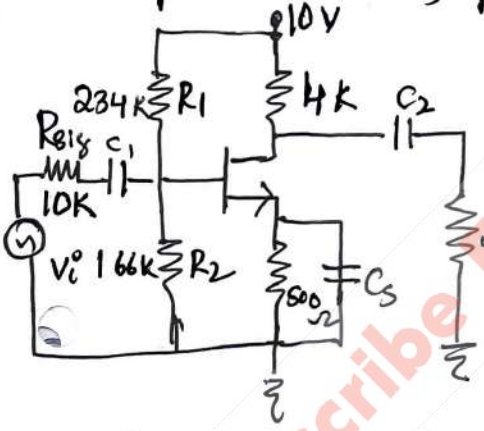
$R_{eq} = R_D \| R_L$

$$f_{Ho} = \frac{1}{2\pi (R_D \| R_L) C_{mo}}$$

$$\omega_{Ho} = \frac{1}{(R_D \| R_L) C_{mo}}$$

∴ High Freq $= F_H = \min (F_{Hi}, F_{Ho})$

(1) Find the high Freq of the MOSFET Amplifier where $C_{gd} = 0.1\,pf$, $C_{gs} = 1\,pF$ & $K = 0.5\,mA/V^2$, $V_t = 2V$, $g_m = 1.55m$



(i) $F_{Hi} = \frac{1}{2\pi (R_{si} \| R_m) C_{gs} + C_{mi}'} = \frac{1}{2\pi R_{eq} C_{eq}}$

$C_{mi} = C_{gd}(1+A)$

$C_{mi}' = 0.1P(1+5.16)$

$C_{mi}' = 0.61PF$

$A = -g_m (R_D \| R_L)$

$A = -1.55m (4K \| 20K)$

$A = -5.16$

-ve sign indicates 180° phase shift.

$g_m = \frac{i_d}{V_{GS}} = 0.25m$

$i_d = \frac{V_{DD} - V_{DS}}{R_D} = 0.835mA$

$V_{DS} = V_D + V_S$

$3.33 + 3.33$

$V_{DS} = 3.$

$i_d = \frac{(10-6.66)}{4K}$

$i_d = K(V_{GS} - V_t)^2$

$0.835m = 0.5m (V_{GS} - 2)^2$

$1.67 = (V_{GS} - 2)^2$

$V_{GS} = 3.29$ $1.29 = V_{GS} - 2$

$C_{eq} = C_{gs} + C_{mi}' = 1PF + 0.61PF$

$C_{eq} = 1.61PF$

$R_{eq} = R_{si} \| R_1 \| R_2$

$10K \| 234K \| 166K$

$R_{eq} = 9.065\,K$ 97K

$R_{eq} = R_D \| R_L$

$= 4K \| 20K$

$R_{eq} = 3.3K$

$F_{Hi} = \frac{1}{2\pi \times 9.865K \times 1.61P}$

$F_{Hi} = 10.9\,MHz$

(2) $F_{Ho} = \frac{1}{2\pi (R_D \| R_L) C_{mo}} = \frac{1}{2\pi R_{eq} C_{eq}}$

$C_{mo} = C_{gd}(1+1/A)$

$= 0.1P(1+\frac{1}{5.16})$

$C_{mo} = 0.12PF$

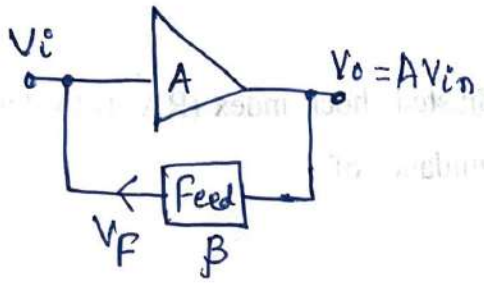
$F_{Ho} = \frac{1}{2\pi (3.3K) \times 0.12PF} =$

$F_{Ho} = 438.44\,MHz$

$F_H = \min (F_{Hi}, F_{Ho}) = 10.9\,MHz$

Introduction to oscillators:

→ Also known as Generators → produce oscillations of particular freq
  ↳ Sustained oscillation
→ without input, generates oscillating o/p.
→ Ex:- Clock signal, audio & radio freq
→ Oscillator Consist of Amplifier & Feedback



$V_F = \beta V_o$

$V_F = \beta (A V_{in})$

$\boxed{V_F = A\beta V_{in}}$

$A\beta$ → loop gain
↳ very imp for producing - oscillations

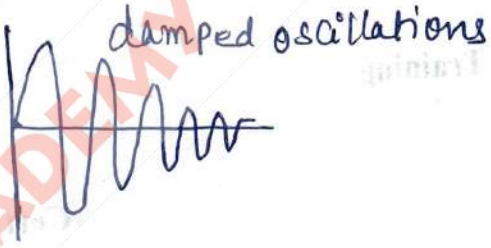
(i) $A\beta < 1$

Ex:- $A\beta = 0.99$ $V_{in} = 2V$

$V_F = 0.99 \times 2V$

$\boxed{V_F = 1.98V}$

Feedback reduces
∴ Vo will also reduces



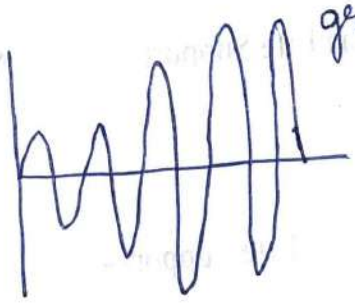
(ii) $A\beta > 1$

Ex:- $A\beta = 1.1$ V_{in} 2V

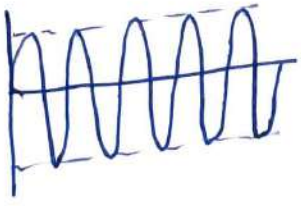
$V_F = 1.1 \times 2V$

$\boxed{V_F = 1.98V}$

Feedback increases
∴ Vo will also increase



To get Sustained oscillations (iii) $A\beta = 1$



Barkhausen Criterion

It explains two conditions to obtain sustained oscillations

(i) $A\beta = 1$ ↛ loop gain = 1

(ii) phase difference b/w i/p & o/p should be 0° (or) 360°

$\angle A\beta = 0°$ (or) $360°$

Working of Practical Oscillator

↛ oscillator does not have i/p, it works without any input connected to it.

even for $V_{in} = 0$ the oscillator will produce o/p (oscillations)

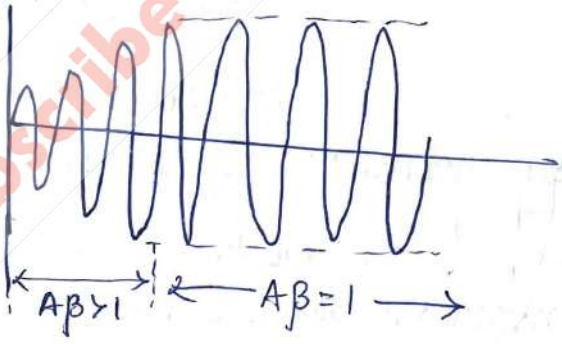
↛ Oscillator should satisfy barkhausen Criterion

(i) $A\beta = 1$ & $\angle A\beta = 0°$ (or) $360°$

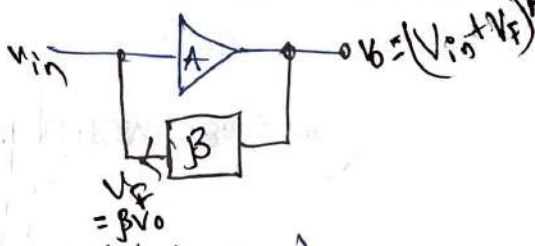
↛ Thermal noise will act as i/p

↛ Initially $A\beta > 1$ ↛ this will help thermal noise to build over the time

↛ Once the required amplitude is obtained then $A\beta = 1$



Mathematical derivation



$V_o = A(V_f + V_{in})$

$V_f = \beta V_o$

$V_o = A(\beta V_o + V_{in})$

$V_o = A\beta V_o + AV_{in}$

$V_o - A\beta V_o = AV_{in}$

$V_o(1 - A\beta) = AV_{in}$

$\because V_{in} = 0$ for oscillators

$1 - A\beta = 0$

$A\beta = 1$ Barkhausen Criterion.

Oscillators → Phase shift → Resistor & Capacitor → RC phase shift osc.

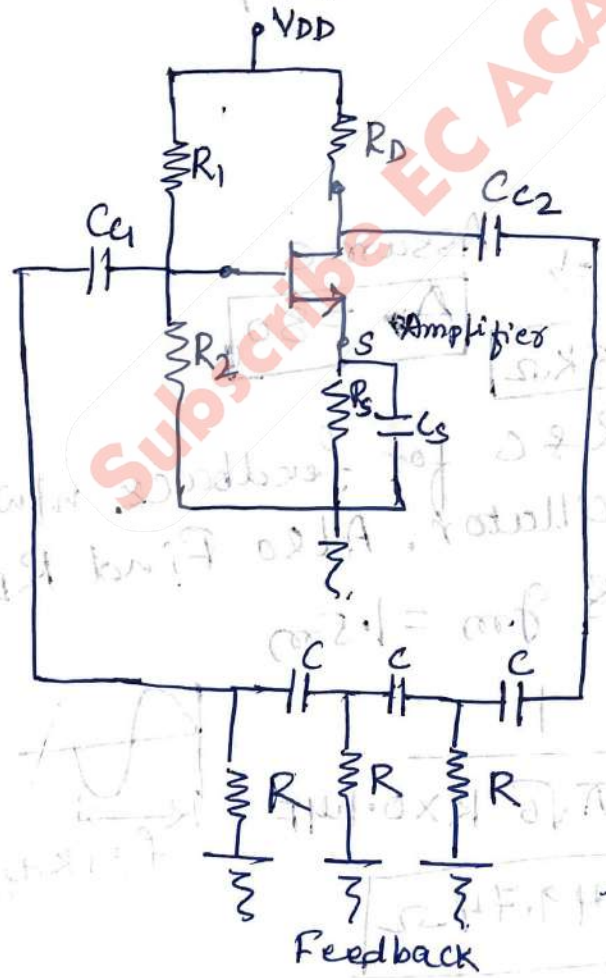
→ LC oscillator → Inductor & Capacitor

Hartley, Crystal, Colpitts, Miller.

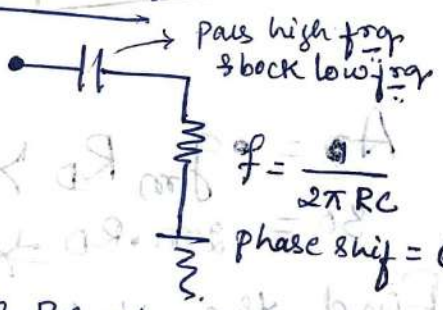
Discuss following w.r.t. oscillators

1. Circuit
2. Operation [Feedback n/w]
3. Formula for oscillator frquency
4. Gain ($A\beta$)
5. phase shift. (Amp = 180° & Feedback = 180°)

I. RC Phase shift OSCillator - FET:



Operation :-



3 RC n/w ⇒ 60° + 60° + 60° = 180°

$$F = \frac{1}{2\pi\sqrt{2N}RC}$$

N → no RC n/w used

here N = 3

$$F = \frac{1}{2\pi\sqrt{6}RC}$$

→ All the resistors & capacitors in feedback are same R & C

gain :- here $\beta = \frac{1}{29}$

$|A\beta| > 1$

$\therefore |A| > 29$

$g_m R_D > 29$ → for oscillations.

phase shift :- Amplifier = 180° & FB = 180° ⇒ 360° (or) 0°

Problem :-

(1) In a RC phase shift oscillator, Feedback n/w uses R = 4.7K & C = 0.47μF & g_m = 2m℧, Find frq of oscillation & gain of the circuit & R_D

$$F = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6} \times 4.7K \times 0.47\mu}$$

$F = 29.41$ Hz

$A_v = g_m R_D > 29 \Rightarrow$ Assume $A_v = 30$

$30 = 2m \cdot R_D \Rightarrow R_D = 15K\Omega$

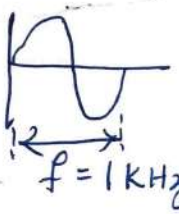
(2) Find the values of R & C for feedback n/w of RC phase shift oscillator. Also Find R_D for frq of 1KHz & g_m = 1.5m℧

$$F = \frac{1}{2\pi\sqrt{6}RC} \Rightarrow 1K = \frac{1}{2\pi\sqrt{6}R \times 0.1\mu F}$$

$R = 649.74\Omega$

Assume any one either R (or) C in KΩ in μF

Assume $C = 0.1\mu F$



21) $|A| > 29$

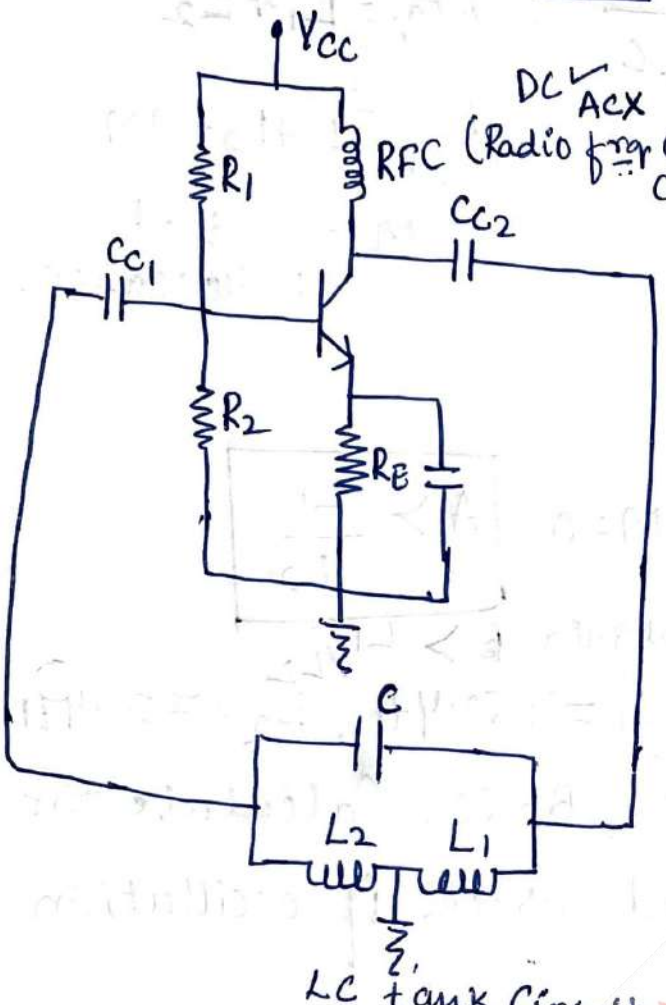
$|g_m R_D| > 29$

$|A| = |g_m R_D|$

$30 = 1.5m \times R_D$

$\boxed{R_D = 20K\Omega}$

Hartley Oscillator - BJT :-



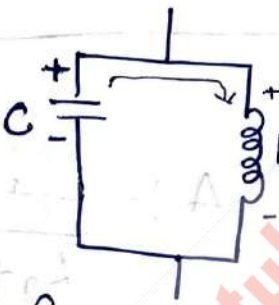
LC tank Circuit.

DC ✓ AC ✗

→ type of LC Oscillator

L - Stores Energy in Magnetic field

C - Store Energy in Electro-Static field.

① 

Resonant ckt
L Tuned ckt.
LC ckt.

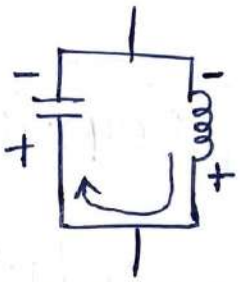
→ Capacitor is fully Charged

→ then it starts discharging and Inductor is charged

→ Inductor Creates magnetic field.

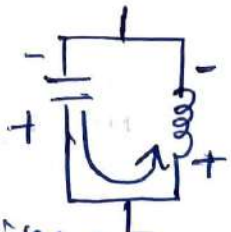
→ Energy in the inductor increases & Capacitor energy decreases.

→ Inductor back Emf & starts discharging & Capacitor Charges.

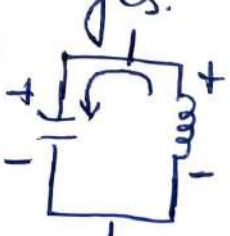
② 

→ Inductor Energy decreases & Capacitor energy increases

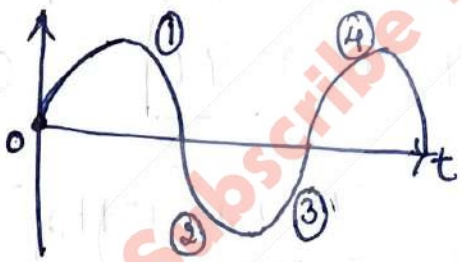
→ Again Capacitor discharges & Inductor Charges.

③ 

Capacitor fully discharge.

④ 

Back Emf & Capacitor Charges & discharges



Wave form.

Frequency $F = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{L_{eq}C}}$

$$\boxed{F = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}}$$

$L_{eq} = L_1 + L_2$

(or)

$L_{eq} = L_1 + L_2 + 2M$

M → mutual Inductance.

gain :- $A > \frac{L_1+M}{L_2+M}$ if $M=0$ $\boxed{A > \frac{L_1}{L_2}}$

Current gain $\beta > L_1/L_2$

(1) In Hartley oscillator $L_1 = 750\mu H$, $L_2 = 750\mu H$ $M = 150\mu H$ & $C = 150\,pf$, $\beta = 50$. Calculate the freq of oscillation and check if oscillation Condition Satisfies.

$$F = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

$L_{eq} = L_1 + L_2 + 2M$

$= 750\mu + 750\mu + 300\mu$

$\boxed{L_{eq} = 1800\mu H}$

$$F = \frac{1}{2\pi\sqrt{1800\mu \times 150p}} \Rightarrow \boxed{F = 306.25\,KHz}$$

$\beta > \frac{L_1+M}{L_2+M} \Rightarrow 50 > \frac{750\mu + 150\mu}{750\mu + 150\mu}$

$\boxed{50 > 1}$

it Satisfies the oscillation Condition.

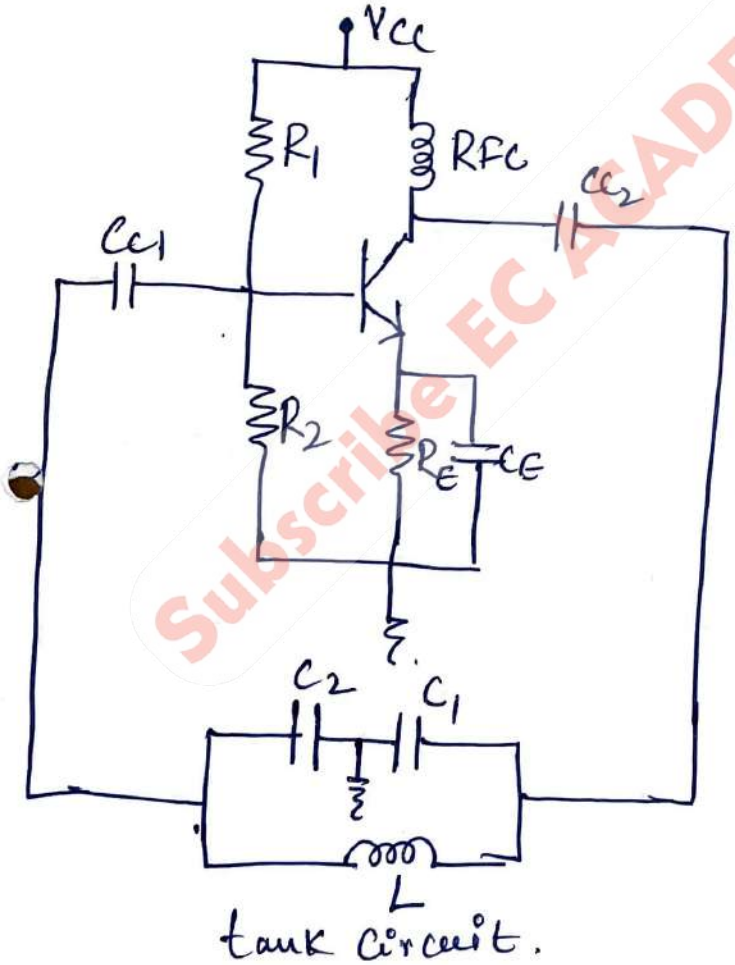
(2) In Hartley oscillator $L_1 = 10\mu H$, $L_2 = 10\mu H$. Find the value of C required for an oscillating freq of 150 KHz.

$$F = \frac{1}{2\pi\sqrt{L_{eq}C}} \Rightarrow F^2 = \frac{1}{4\pi^2 L_{eq} C}$$

$$C = \frac{1}{4\pi^2 F^2 L_{eq}} \Rightarrow C = \frac{1}{4\pi^2 \times (150K)^2 \times (10\mu + 10\mu)}$$

$$\boxed{C = 56.28\ nF}$$

Colpitts Oscillator



$$F = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

$$\boxed{C_{eq} = \frac{C_1 C_2}{C_1 + C_2}}$$

$$\boxed{A > \frac{C_2}{C_1}}$$

$$\boxed{h_{fe} = \beta > \frac{C_2}{C_1}}$$

Current gain

(1) In Colpitts oscillator, $C_1 = 1nF$, $C_2 = 99nF$, $L = 1.5mH$, & $\beta_{(hfe)} = 110$. Calculate the freq of oscillation & Check the Condition for oscillation.

$$F = \frac{1}{2\pi\sqrt{L C_{eq}}} \qquad C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{(1n)(99n)}{(1n)+(99n)}$$

$$C_{eq} = 0.99nF.$$

$$F = \frac{1}{2\pi\sqrt{(1.5m)(0.99nF)}} \Rightarrow \boxed{F = 130.6KHz}$$

$$\beta > \frac{C_2}{C_1} \Rightarrow 110 > \frac{99nF}{1nF}$$

$\boxed{110 > 99}$ Condition is satisfied.

(2) In Colpitts oscillator $C_1 = C_2 = C$ & $L = 100\mu H$, the freq of oscillator is 500 KHz. Determine the Value of C

$$F = \frac{1}{2\pi\sqrt{L C_{eq}}} \qquad C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{C^2}{2C}$$

$$F^2 = \frac{1}{4\pi^2 L C_{eq}} \qquad C_{eq} = \frac{C}{2}$$

$$C = 2C_{eq} \Rightarrow \boxed{C = 2.026nF}$$

$$C_{eq} = \frac{1}{4\pi^2 L F^2} = \frac{1}{4\pi^2(100\mu)(500K)^2}$$

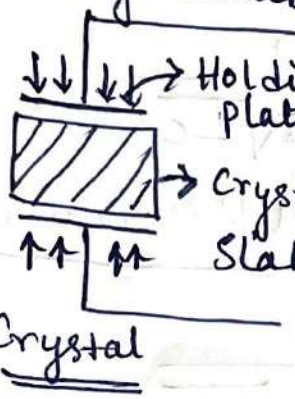
$$C_{eq} = 1.0132nF$$

$\boxed{n \to 10^{-9}}$

Crystal Oscillator :-

→ Naturally Crystal is in Hexagonal prism
→ but it is cut into rectangular shap for practical use

→ Natnally available Crystal



→ It works on the principle of "Piezoelectric effect".

→ When a Crystal is mechanically Vibrated

→ The a.c. Voltage get generated across opposite faces of the Crystal.

→ Every crystal has its own resonating freq

→ Hence under the influence of the mechanical Vibrations, the crystal generates an electrical signal of very const freq.

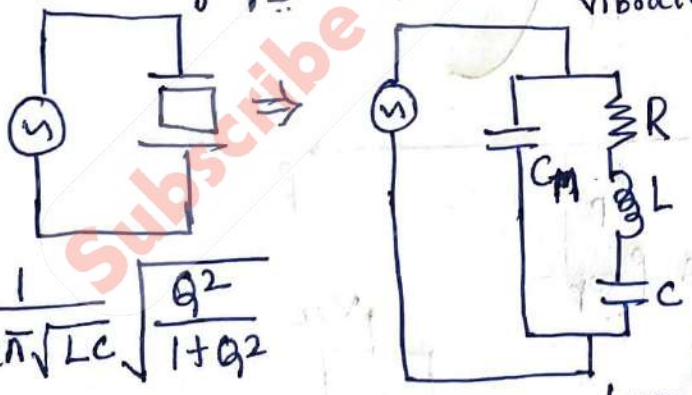
$$f \propto \frac{1}{\text{thickness}}$$

→ Crystal is very much stable in holding the Constant freq.

→ Commonly used Crystal is Quartz Crystal → mechanically strong, good piezo electric, less expnsive.

AC equivalent Ckt :-

f_r → Resonating freq → natural freq, where a medium vibrates at high amplitude



C_M → mounting Capacitance
↳ It is the Capacitance in the Crystal b/w two parallel plates.

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}}$$

Q → Quality factor of Crystal

here $Q = \frac{\omega L}{R}$

R → is the resistance due to internal friction while Crystal is vibrating

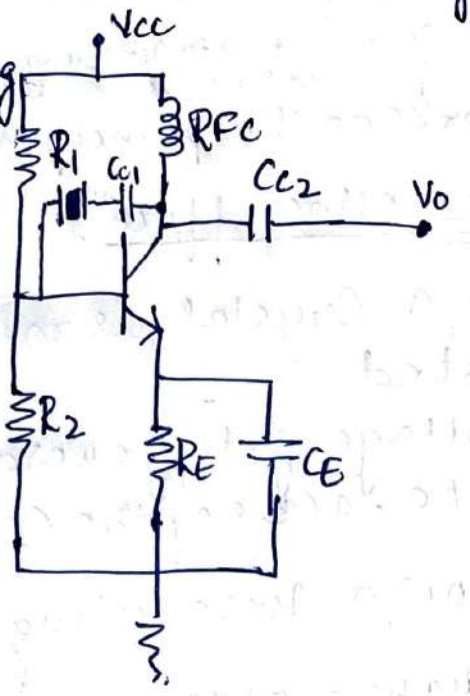
L → Mass of Crystal which is indication of inertia

C → Stiffness is represented as Capacitor.

∵ Q = 20,000 (typical value) then $\sqrt{\frac{Q^2}{1+Q^2}} \approx 1$

∴ $f_r = 1/2\pi\sqrt{LC}$

Series Resonating Circuit.



Two types of Resonance

(i) Series Resonance

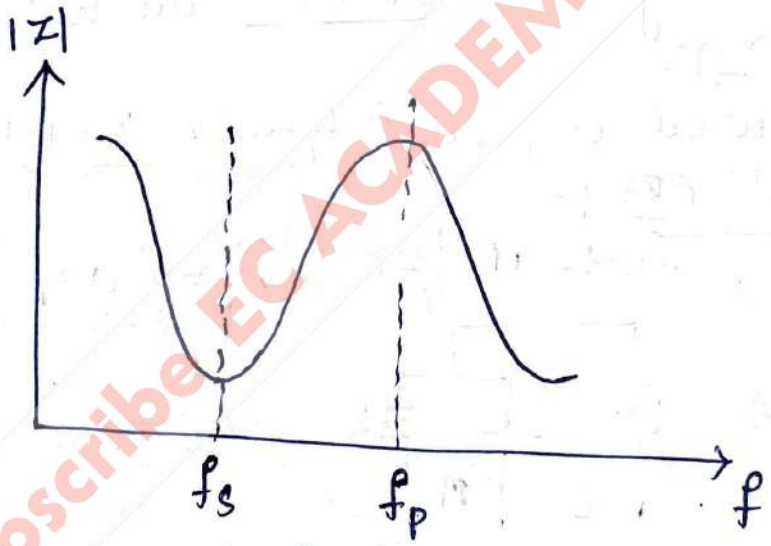
$$F_s = \frac{1}{2\pi\sqrt{LC}}$$

(ii) Parallel Resonance

$$F_p = \frac{1}{2\pi\sqrt{L\,C_{eq}}}$$

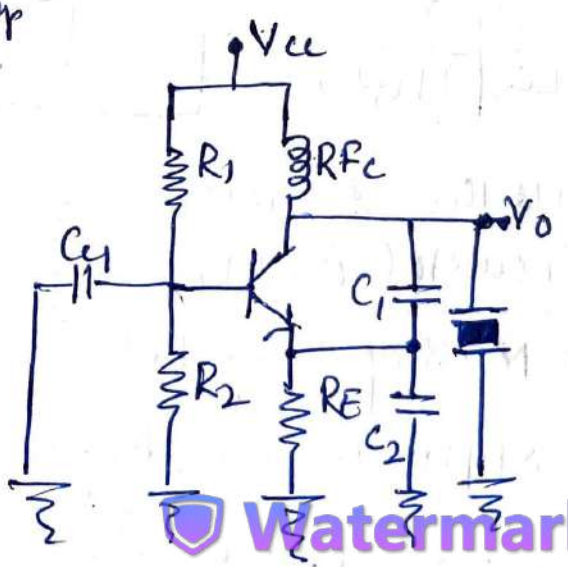
$$C_{eq} = \frac{C_{mn}C}{C_{mn}+C}$$

Feedback n/w



|Z| V/s f_{resp}

Parallel Resonating Ckt



① A Crystal has $L=0.4H$, $C=0.085PF$ & $C_m=1PF$ with $R=5K\Omega$. Find (i) Series Resonent freq (ii) parallel Resonent freq (iii) By what percentage does the Parallel Resonent freq exceed the Series Resonent freq? (iv) Find Q-factor of Crystal.

Soln :- (i) $f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.4\times0.085\times10^{-12}}} = 863.138KHz$

(ii) $C_{eq} = \frac{CC_m}{C+C_m} = \frac{0.085\times1.}{0.085+1} = 0.0783PF$

$\therefore f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.4\times0.0783\times10^{-12}}} = 899.074$ KHz

(iii) % increase $= \frac{899.074-863.138}{863.138}\times100 = 4.163\%$

(iv) $Q = \frac{W_sL}{R} = \frac{2\pi f_sL}{R} = \frac{2\pi\times863.138\times10^3\times0.4}{5\times10^3} = 433.86$

② A Crystal has mounting Capacitance of 10PF. The inductance equivalent of mass is 1mH, the frictional resistance is $1K\Omega$ Compliance is 1PF. Find series & parallel Resonant freq

(i) $F_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{1\times10^{-3}\times1\times10^{-12}}} = 5.033MHz$

(ii) $C_{eq} = \frac{CC_m}{C+C_m} = \frac{1\times10^{-12}\times10\times10^{-12}}{1\times10^{-12}+10\times10^{-12}} = 9.0909\times10^{-13}F$

$$f_p = \frac{1}{2\pi\sqrt{L C_{eq}}} = \frac{1}{2\pi\sqrt{1\times10^{-3}\times9.0909\times10^{-13}}}$$

$$f_p = 5.2785 \text{ MHz}$$

AEC

21EC34

Module-3

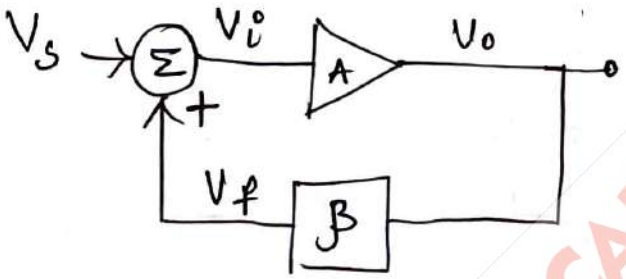
Feedback Network

→ Connecting Amplifier & Feedback [redacted] together and giving i/p to obtain o/p.

→ difference b/w Feedback n/w & oscillator is that in oscillator no i/p is given, but in feed n/w we give i/p.

→ Two types → Positive Feedback n/w (i/p signal & part of o/p signal are in phase.)
→ Negative Feedback n/w (i/p signal & part of o/p signal are out of phase.)

Positive FB n/w :-



V_o → o/p v+g $= A V_i$

A → gain of Amplifier (without FB)

β → gain of F.B. n/w

V_f → o/p v+g of F.B. n/w

$V_f = \beta V_o$

A_f → gain with feedback

V_i → error signal (i/p v+g)

$V_i = V_s + V_f$

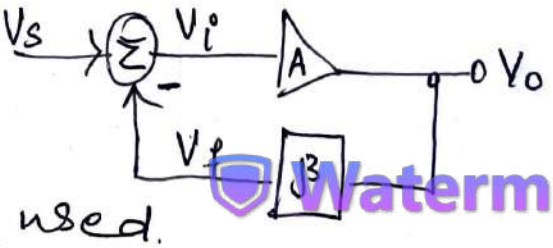
$$A_f = \frac{V_o}{V_s} = \frac{AV_i}{V_i - V_f} = \frac{AV_i}{V_i - \beta V_o}$$

$$A_f = \frac{AV_i}{V_i - \beta A V_i} \Rightarrow A_f = \frac{V_i(A)}{V_i(1 - A\beta)}$$

$$\boxed{A_f = \frac{A}{1 - A\beta}}$$

Negative feedback

→ most Commonly used.



here, $V_i = V_s - V_f$

$$A_f = \frac{V_o}{V_s} = \frac{AV_i}{V_i + V_f} = \frac{AV_i}{V_i + \beta V_o} = \frac{AV_i}{V_i + \beta A V_i}$$

$$A_f = \frac{\cancel{V_i}(A)}{\cancel{V_i}(1+A\beta)} \Rightarrow \boxed{A_f = \frac{A}{1+A\beta}}$$

Problems:-

① For a non inverting opamp shown in figure.

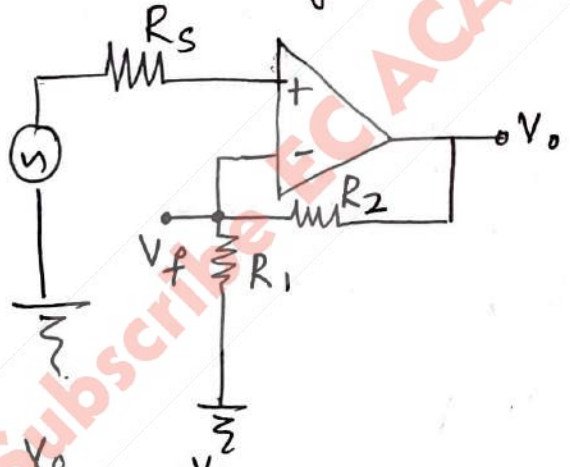
(a) Find β equation using R-n/w

(b) Find β; where $A = 10^4$ & $A_f = 10$

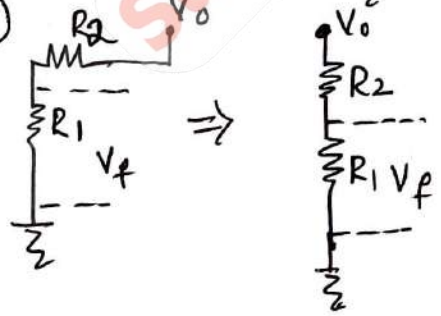
(c) what is β in dB?

(d) if $V_s = 1V$ find V_o, V_f & V_i

(e) 'A' reduced by 20%. what is Change in A_f.



(a)



Vtg divider rule

$$V_f = \frac{R_1}{R_1+R_2} V_o$$

$$\beta = \frac{V_f}{V_o} = \frac{\frac{R_1}{R_1+R_2}\cancel{V_o}}{\cancel{V_o}}$$

$$\boxed{\beta = \frac{R_1}{R_1+R_2}}$$

(b) $A_f = \frac{A}{1+A\beta}$

$10 = \frac{10^4}{1+10^4\beta} \Rightarrow$ **$\beta = 0.0999 \simeq 0.1$**

(c) β in dB $= 20 \log \beta = 20 \log 0.0999$

$\beta_{dB} = -20$

(d) $V_s = 1$ $\quad V_o = A V_i$ (or) $V_o = A_f V_s$

V_i not given $\quad V_o = 10 \times 1$

$V_o = 10V$

$V_f = \beta V_o = 0.0999 \times 10$

$V_f = 0.999\,V$

$V_i = V_s - V_f = 1 - 0.999V$

$V_i = 0.1mV$

(e) $A = 10^4$

$A' = A - 20\%$ of A

$A' = 10^4 - 2000$

$A' = 80,000$

$A_f = \frac{A'}{1+A'\beta} = \frac{80,000}{1+80,000 \times 0.0999}$

$A'_f = 9.997$

$A_f = 10$

% Change in $A_f = \frac{A_f - A_f'}{A_f'} \times 100\%$

$= \frac{10 - 9.997}{9.997} \times 100\%$

% Change in $A_f = 0.02\%$

What is Feedback amplifier?

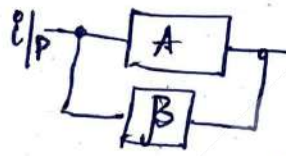
→ Taking the portion of o/p signal and feeding it back to i/p of an Amplifier.

Why Feedback amplifier?

→ To increase the Band width.
→ Reduce the noise effect
→ Linearity of gain.

Disadvantage:

→ Reduces the gain.
→ Complex
→ Costly.



A_f → Reduces as β value increase.

$A_f = \frac{A}{1+A\beta}$ if $A\beta >> 1$

$A_f = \frac{A}{A\beta} \Rightarrow \boxed{A_f = \frac{1}{\beta}}$

Gain de-sensitivity → Ratio of differential gain to total gain.

$= \frac{dA_f}{A_f}$ ∵ $A_f = \frac{A}{1+A\beta}$ for negative Feedback.

differentiate w.r.t gain A.

$$\frac{dA_f}{dA} = \frac{1}{(1+A\beta)^2} = \boxed{dA_f = \frac{dA}{(1+A\beta)^2}}$$

$$\therefore \frac{dA_f}{A_f} = \frac{\frac{dA}{(1+A\beta)^2}}{\frac{A}{1+A\beta}} = \frac{dA}{(1+A\beta)^2} \times \frac{(1+A\beta)}{A}$$

$$\boxed{\frac{dA_f}{A_f} = \frac{1}{1+A\beta} \times \frac{dA}{A}}$$

$\frac{1}{1+A\beta}$ → desensitivity amount.

Reciprocal of sensitivity is Desensitivity $D = 1+A\beta$

Basic types of feedback amplifier (negative feedback)

i/p → V (or) I o/p → V (or) I.

i/p	o/p	gain (A)
Voltage (Series)	Voltage (Shunt)	V-tg gain $A_V = V_o/V_i$
Current (Shunt)	Voltage (Shunt)	$\frac{V}{I}$ → Resistance gain $R_m = V_o/I_i$
Voltage (Series)	Current (Series)	$\frac{I}{V}$ → Trans Conductance gain $g_m = I_o/V_i$
Current (Shunt)	Current (Series)	current gain $A_I = I_o/I_i$

i/p	o/p	Connection
V-tg	current	→ Series
Current	V-tg	→ Shunt

Series-Shunt Amplifier ⇒ Voltage-Series Feedback amplifier (o/p type, i/p connection)

Shunt-shunt Amplifier ⇒ Voltage-shunt Feedback Amplifier

Series-Series Amplifier ⇒ Current-Series Feedback Amplifier

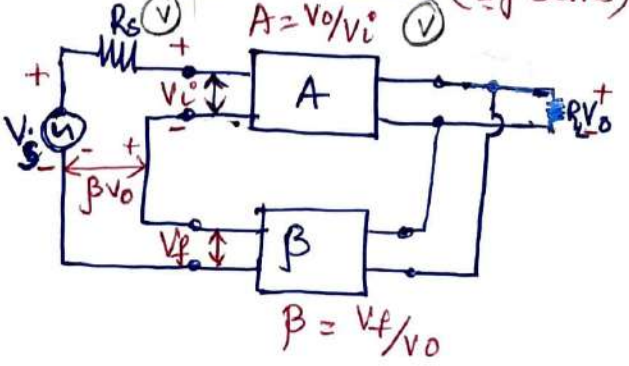
Shunt-Series Amplifier ⇒ Current-Shunt Feedback amplifier

Method for feedback Amplifier Analysis:

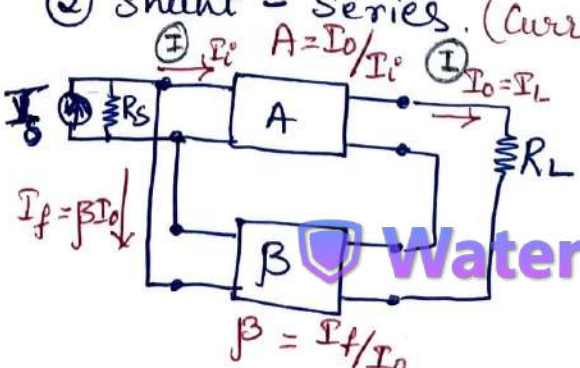
→ Recognizing the Feedback Amplifier Ckt.
→ Calculate the gain 'A' → Amplifier gain.
→ Calculate the feedback gain 'β'
→ Calculate gain with Feedback $A_f = \frac{A}{1+A\beta}$
→ Calculate i/p & o/p resistance.

Block diagram of Feedback Amplifier. (Topologies)

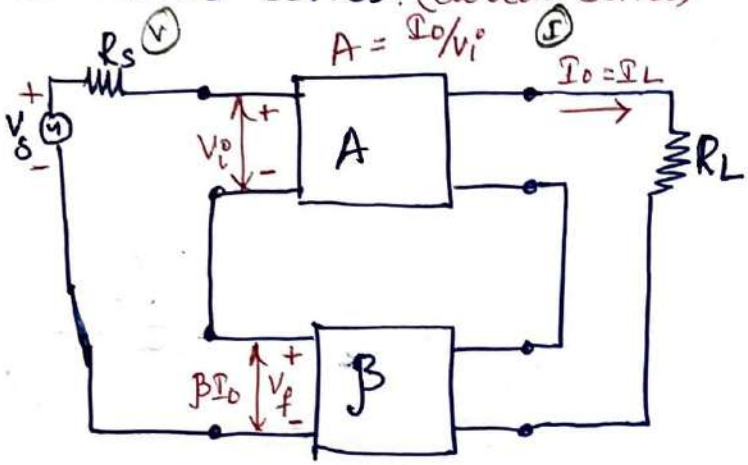
① Series-Shunt (V-tg Series)



② Shunt-Series. (Current-Shunt)



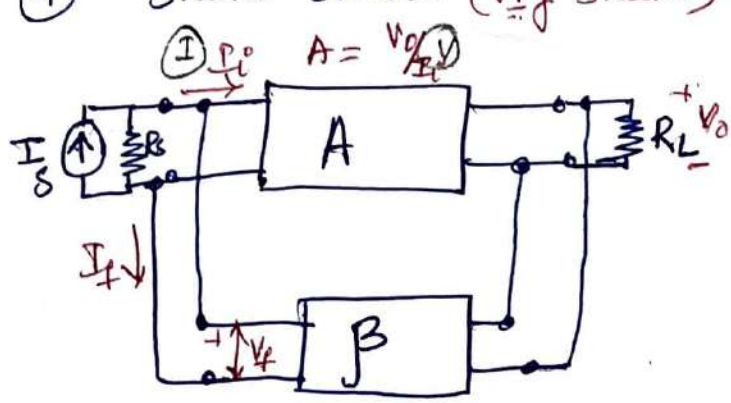
③ Series - series (Current Series)



$A = I_o / V_i$

$\beta = V_f / I_o$

④ Shunt - Shunt (V+g Shunt)



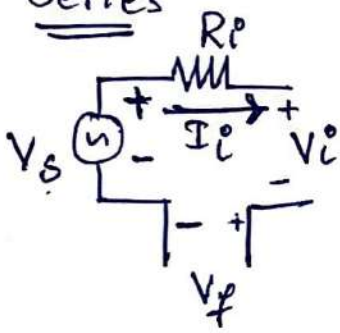
$A = V_o / I_i$

$\beta = I_f / V_o$

To find i/p resistance & o/p resistance.

i/p Resistance

Series



$R_i = V_i / I_i$

$R_{if} = V_s / I_i$

Apply KVL

$V_s - V_i - V_f = 0$

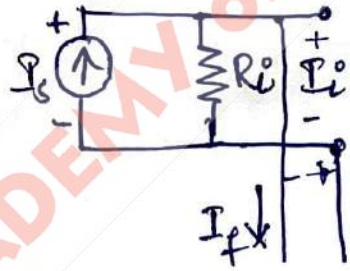
$\boxed{V_s = V_i + V_f}$

$V_s = I_i R_i + \beta V_o$ (or) I_o

$V_s = I_i R_i + \beta A V_i \rightarrow I_i R_i$

$\therefore \boxed{R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta A)}$

Shunt



$R_i = V_i / I_i$

$R_{if} = V_i / I_s$

Apply KCL

$I_s - I_i - I_f = 0$

$\boxed{I_s = I_i + I_f}$

$I_s = \frac{V_i}{R_i} + \beta V_o$

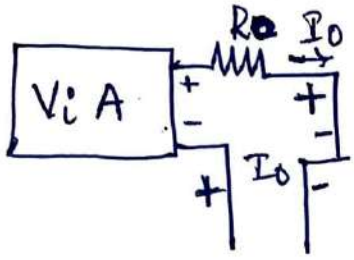
$I_s = V_i / R_i + \beta A I_i \rightarrow V_i / R_i$

$I_s = V_i / R_i + \beta A V_i / R_i$

$\boxed{R_{if} = \frac{V_i}{I_s} = R_i / 1 + \beta A}$

o/p Resistance

Series



$V_s = 0$ ----> to find o/p Resistance

$V_i = V_s - V_f$

$V_i = -V_f$

$$\boxed{V_i = -\beta I_o}$$

$$R_{of} = \frac{V_o}{I_o}$$

Apply KCL

$$V_i A + \frac{V_o}{R_L} - I_o = 0$$

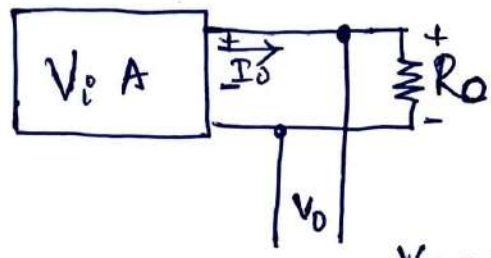
$$V_o = (-V_i A + I_o) R_o$$

$$V_o = (\beta I_o A + I_o) R_o$$

$$R_{of} = \frac{V_o}{I_o} = \frac{(\beta I_o A + 1) I_o R_o}{I_o}$$

$$\boxed{R_{of} = R_o (1 + \beta A)}$$

Shunt



Apply KVL

$V_s = 0$

$V_i = V_s - V_f$

$V_i = -V_f$

$V_i = -\beta V_o$

$$I_o = \frac{V_o - V_i A}{R_o}$$

$$I_o = \frac{V_o + V_f A}{R_o}$$

$$I_o = \frac{V_o + \beta V_o A}{R_o}$$

$$R_{of} = \frac{V_o}{I_o} = \frac{V_o}{\frac{V_o (1 + \beta A)}{R_o}}$$

$$\boxed{R_{of} = \frac{R_o}{(1 + \beta A)}}$$

Feedback	i/p Resistance	o/p Resistance
Series.	$R_i (1 + \beta A)$	$R_o (1 + \beta A)$
Parallel. (Shunt)	$R_i / (1 + \beta A)$	$R_o / (1 + \beta A)$

Problems :-

① For inverting amplifier, if $V_s = 1V$, $V_i = 5mV$ & $V_o = 5V$, find β & open loop gain

$A_f \rightarrow$ Closed loop gain
$A \rightarrow$ open loop gain.

Important formule

$V_o = A V_i$

$V_f = \beta V_o$

$V_i = V_s - V_f$

$A_f = \frac{A}{1 + A\beta}$

$\beta = \frac{V_f}{V_o}$

$\beta = 0.995/5$

$\boxed{\beta = 0.199}$

$V_f = V_s - V_i$

$V_f = 1 - 5m$

$V_f = 0.995$

$A = \frac{V_o}{V_i} = \frac{5V}{5mV} \Rightarrow \boxed{A = 1000}$

② if $1/\beta$ is five times A_f & $A = 1000$ find loop gain & Values of β & A_f.

$5A_f = \frac{1}{\beta}$ $\quad A = 1000$

$A_f = \frac{A}{1 + A\beta} \Rightarrow \beta = \frac{1}{5A_f} \Rightarrow A_f = \frac{1}{5\beta}$

$\frac{1}{5\beta} = \frac{A}{1 + A\beta} \Rightarrow \frac{1}{5\beta} = \frac{1000}{1 + 1000\beta} \Rightarrow$

$1 + 1000\beta = 1000 \times 5\beta$

$1 = 5000\beta - 1000\beta$

$1 = 4000\beta$

$\beta = \frac{1}{4000} = 0.25 \times 10^{-3}$

$\boxed{\beta = 0.00025} \Rightarrow \boxed{\beta = 0.25 \times 10^{-3}}$

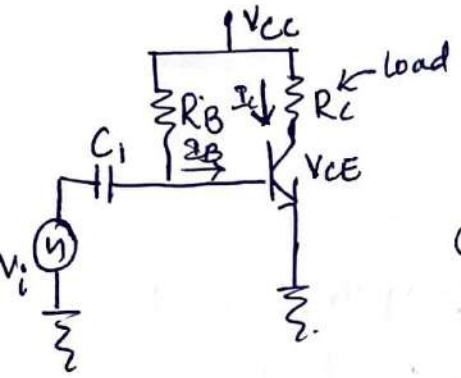
$A_f = \frac{1}{5\beta} = \frac{1}{5 \times 0.00025} \Rightarrow \boxed{A_f = 800}$

Output stage & Power Amplifier:

Power Amplifier → Amplifier amplifies power of the signal

$P = (V \cdot I)$ → Amplified.

D.C. load line:-



o/p side

$V_{CC} - I_C R_C - V_{CE} = 0$

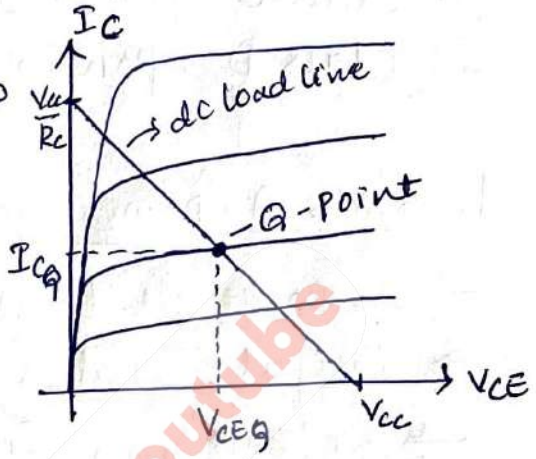
$V_{CE} = V_{CC} - I_C R_C$

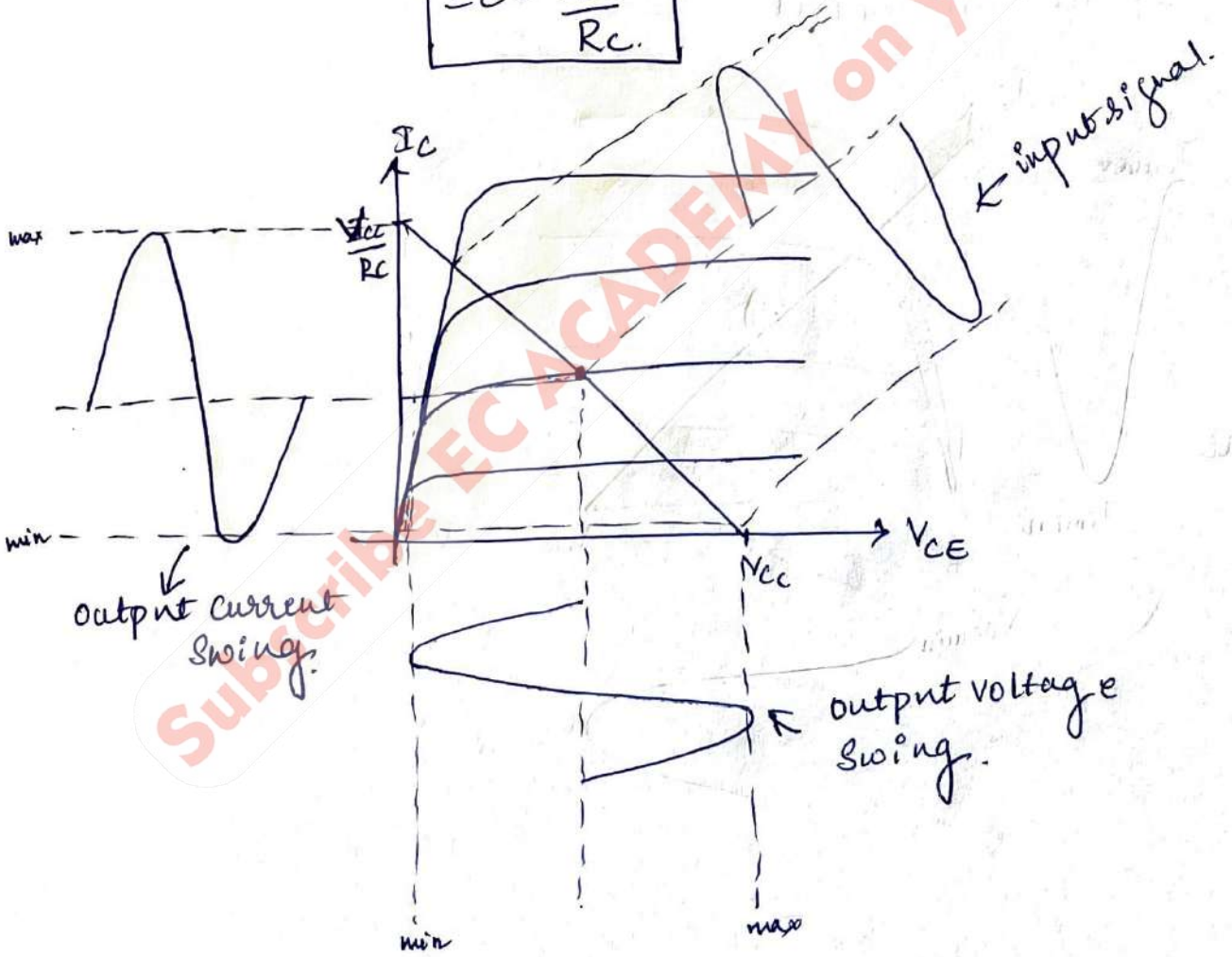
Case(i) $I_C = 0$

$$\boxed{V_{CE} = V_{CC}}$$

Case(ii) $V_{CE} = 0$.

$$\boxed{I_C = \frac{V_{CC}}{R_C}}$$





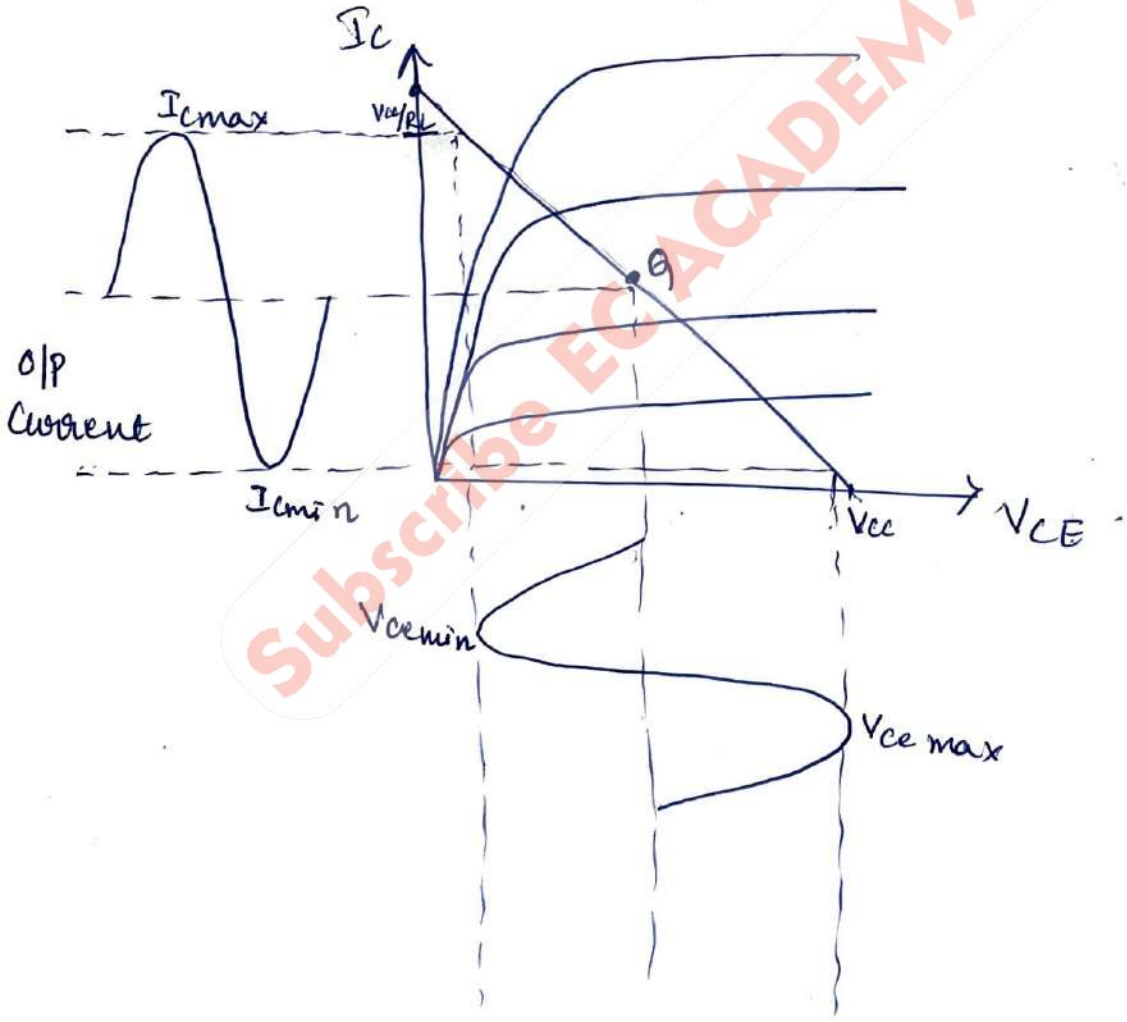
AC operation

Classification of power Amplifiers :-

1. Class A power amplifier → Q-point is at Center of dc load line
2. Class B power amplifier → Q-point at Cutoff region
3. Class AB power amplifier → Q-point b/w Center & Cutoff region above
4. Class C power amplifier → Q-point below Cutoff region.
5. Class D power amplifier.

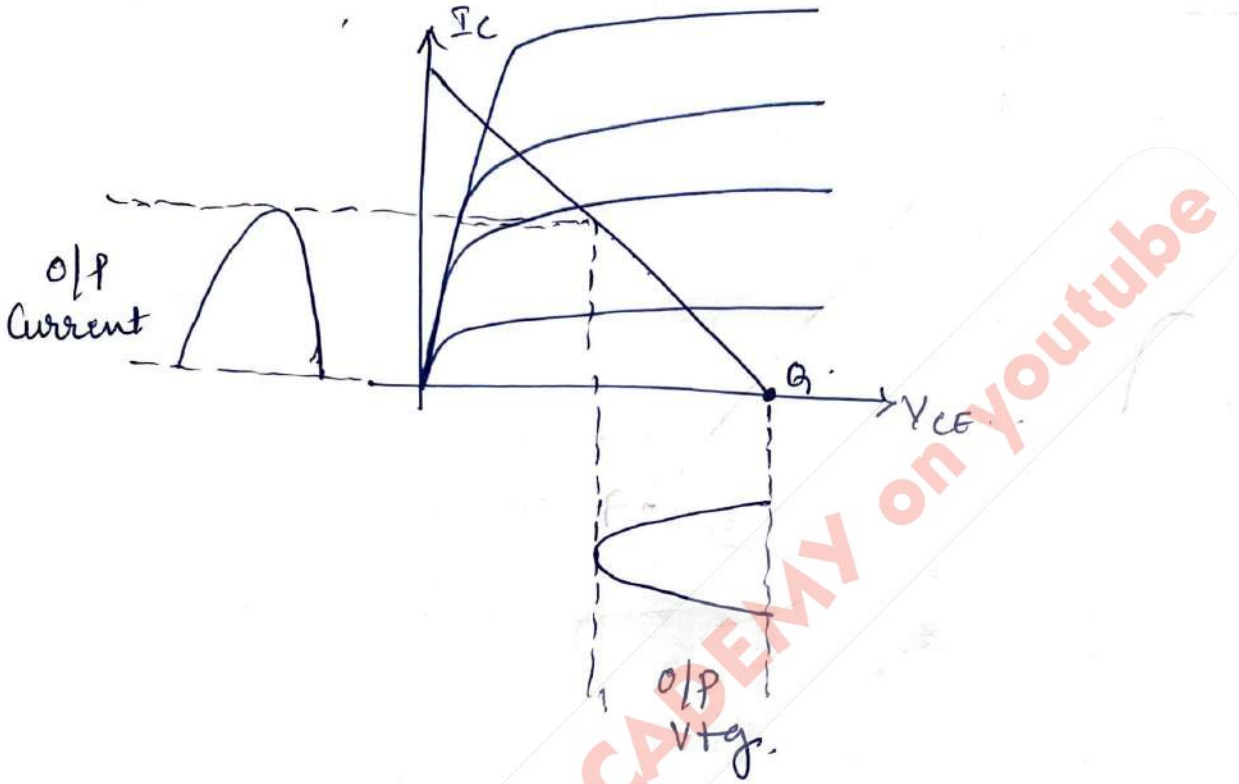
1. Class A power Amplifier :-

→ Q-point is located at the Centre of the load line
→ Output signal varies over full cycle of the i/p signal
→ So collector current flows for 360° (full cycle) of the i/p signal.



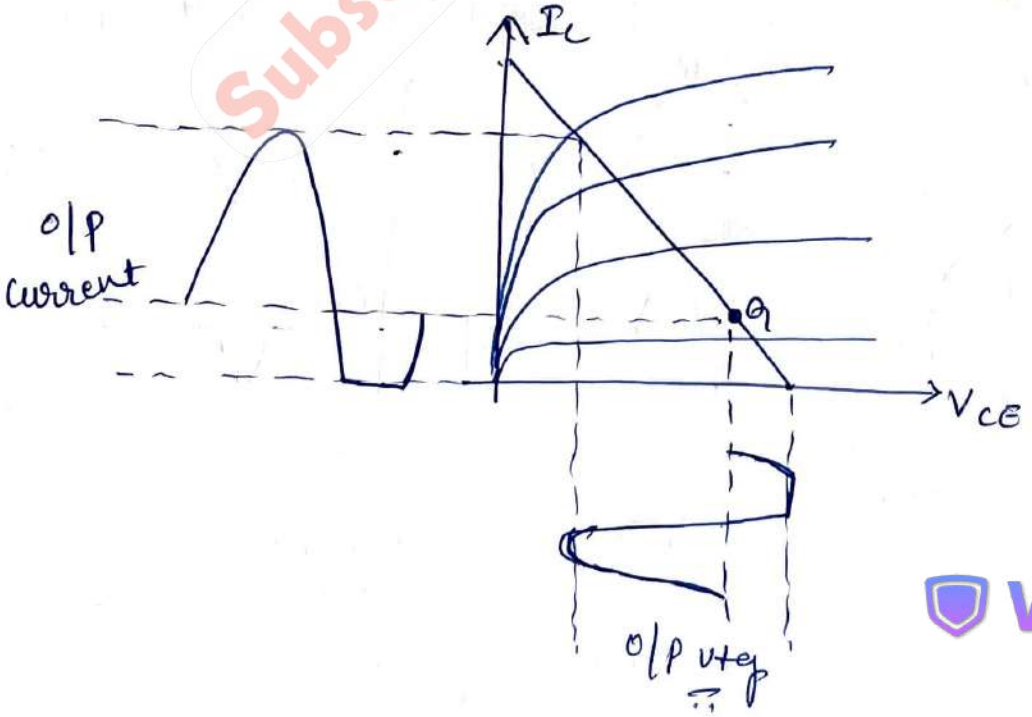
2. Class B Power Amplifier:-

→ Q-point is located at cutoff region of loadline
→ o/p signal varies over one half cycle of i/p signal
→ so collector current flows for 180° (half cycle) of i/p signal.



3. Class AB power Amplifier:-

→ Q-point is selected such that o/p is more than 180° & less that 360° of i/p signal

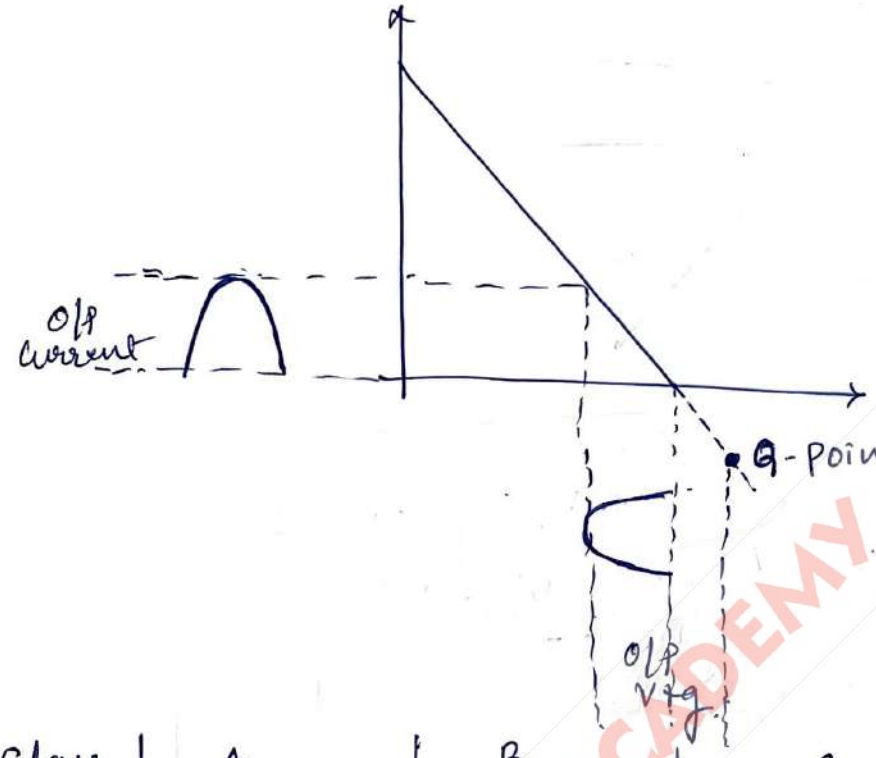


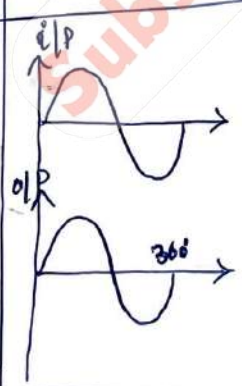
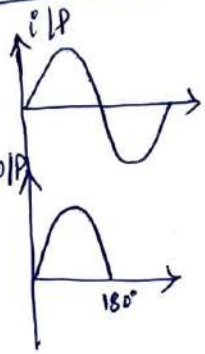
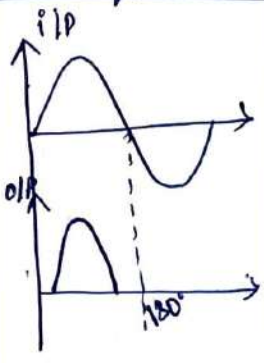
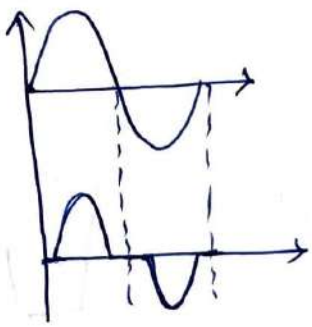
4. Class C power amplifier:-

→ Transistor is biased below cutoff region.

→ The Q-point of the transistor remains in active region for less than half cycle, so only that part is represented at o/p.

→ so collector current flows for less than 180°.

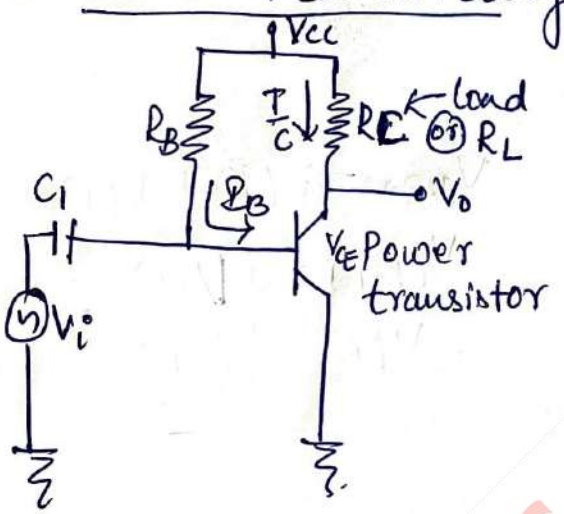


Class.	A	B	C	A-B
Operating cycle	360°	180°	less than 180°	more than 180° less than 360°
Q-Point	Centre of load line	On cutoff region	below cutoff region	Above cutoff region & below centre of load line
I/P-O/P waveform				
Efficiency	Poor 25% to 50%	Better 78.5%	High	More than A & less than B amplifier
Distortion	Absent no distortion	Present	Highest	Present

Calculations :-

1. DC analysis → i/p
2. AC analysis → o/p.
   - → using RMS signal
   - → using peak signal
   - * → using peak-to-peak signal *
   - → using Max & Minimum.
3. Max Efficiency (o/p / i/p)

(1) Series-fed directly coupled Class A Power amplifier :-



→ A simple fixed bias CE is shown in figure.

→ It is used to discuss main features of Class A Series fed amplifier.

→ R_L is load connected in series with collector, so the name Series-fed amplifier

DC Analysis

Apply KVL to o/p side

$$V_{CC} - I_C R_C - V_{CE} = 0$$

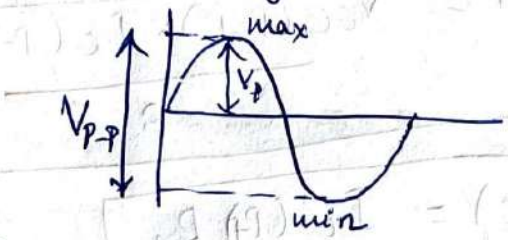
$$\boxed{V_{CC} = I_C R_C + V_{CE}}$$

$$\therefore \boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}}$$

The dc power i/p is

$$\boxed{P_i(dc) = V_{CC} I_{CQ}}$$

AC analysis :-



RMS signals

$$\boxed{\begin{aligned} P_o(ac) &= V_{CE(rms)} I_{C(rms)} \\ P_o(ac) &= I^2_{C(rms)} R_C \\ P_o(ac) &= \frac{V^2_{CE(rms)}}{R_C} \end{aligned}}$$

Using Peak signals

$V_{rms} = \frac{V_m}{\sqrt{2}}$ $I_{rms} = \frac{I_m}{\sqrt{2}}$

$P_{o(ac)} = V_{CE(rms)} \cdot I_{C(rms)}$

$P_{o(ac)} = \frac{V_{CE(P)}}{\sqrt{2}} \cdot \frac{I_{C(P)}}{\sqrt{2}}$

$$P_{o(ac)} = \frac{V_{CE(P)} \cdot I_{C(P)}}{2}$$

$$P_{o(ac)} = \frac{I_{C}^2(P) R_C}{2}$$ → ~~$P_{o(ac)} = \frac{I_{C(max)}}{2}$~~

$$P_{o(ac)} = \frac{V_{CE}^2(P)}{2 R_C}$$

Using Peak to Peak Signals

$V_{(P-P)} = V(P) + V(P)$

$V_{(P-P)} = 2V(P)$

$V(P) = \frac{(V_{P-P})}{2}$

$P_{o(ac)} = V_{CE(rms)} \cdot I_{C(rms)}$

$= \frac{V_{CE(P)}}{\sqrt{2}} \cdot \frac{I_{C(P)}}{\sqrt{2}}$

$= \frac{V_{CE(P)} \cdot I_{C(P)}}{2}$

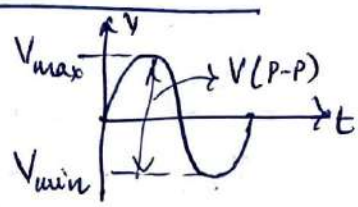
$= \frac{V_{CE(P-P)}/2 \cdot I_{C(P-P)}/2}{2}$

$$P_{o(ac)} = \frac{V_{CE(P-P)} \cdot I_{C(P-P)}}{8}$$

$$P_{o(ac)} = \frac{I_{C}^2(P-P) R_C}{8}$$

$$P_{o(ac)} = \frac{V_{CE}^2(P-P)}{8 R_C}$$

Using maximum & Minimum values



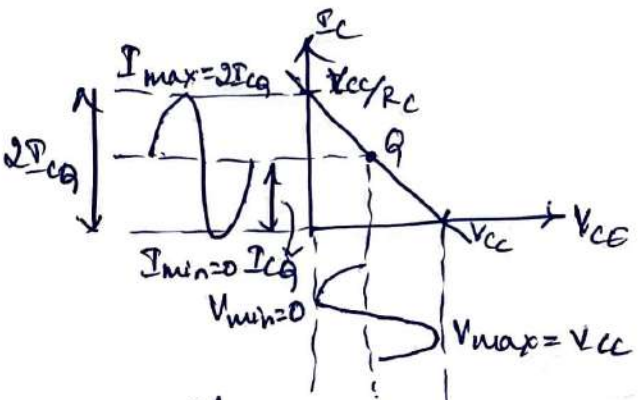
$V_{CE(P-P)} = V_{max} - V_{min}$

$I_{C(P-P)} = I_{max} - I_{min}$.

$P_{o(ac)} = \frac{V_{CE(P-P)} \cdot I_{C(P-P)}}{8}$

$$P_{o(ac)} = \frac{[V_{max} - V_{min}][I_{max} - I_{min}]}{8}$$

Maximum efficiency :-



Class-A amplifier

For maximum efficiency

$V_{max} = V_{cc}$ & $V_{min} = 0$

$I_{max} = 2I_{CQ}$ & $I_{min} = 0$

The dc power i/p is

$$P_i(dc) = V_{cc} I_{CQ}.$$

& ac power o/p is

$$P_o(ac) = \frac{[V_{max} - V_{min}][I_{max} - I_{min}]}{8}$$

$$\therefore \max \%\eta = \frac{\max P_o(ac)}{\max P_i(dc)} \times 100\%$$

$$= \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{cc} \cdot I_{CQ}} \times 100\%$$

$$= \frac{V_{cc} \cdot 2I_{CQ}}{8 V_{cc} \cdot I_{CQ}} \times 100\%$$

$$\boxed{\max \%\eta = 25\%}$$

Transformer Action :-

→ Transformer Converts AC to AC

→ $V_2 > V_1 \Rightarrow$ Step up transformer

→ $V_1 > V_2 \Rightarrow$ Step down transformer.

Votage transformation : $\frac{V_2}{V_1} = \frac{N_2}{N_1}$

Current transformation : $\frac{I_2}{I_1} = \frac{N_1}{N_2}$

Impedence transformation :

$$\frac{R_L}{R_L'} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2 I_1}{V_1 I_2} = \frac{V_2}{I_2} \times \frac{I_2}{I_1} = \frac{N_2}{N_1} \cdot \frac{N_2}{N_1} = \left(\frac{N_2}{N_1}\right)^2$$

$$\therefore \boxed{\frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2} \Rightarrow \frac{R_L'}{R_L} = \left(\frac{N_1}{N_2}\right)^2$$

$$\boxed{R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L}$$

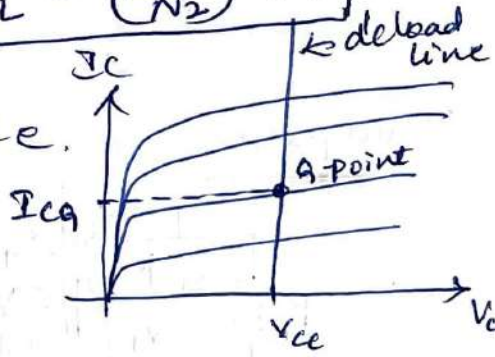
DC operation :-

Apply KVL at Collector side.

$V_{cc} - V_{CE} = 0$

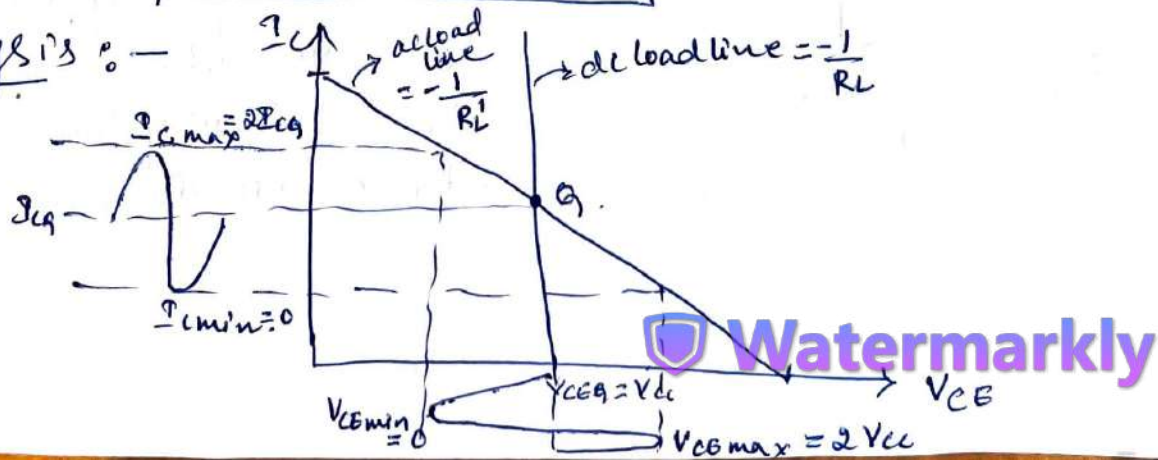
$\therefore V_{cc} = V_{CE}$

$\boxed{V_{CEQ} = V_{cc}}$ - This is dc bias V to q V_{CEQ} for transistor.



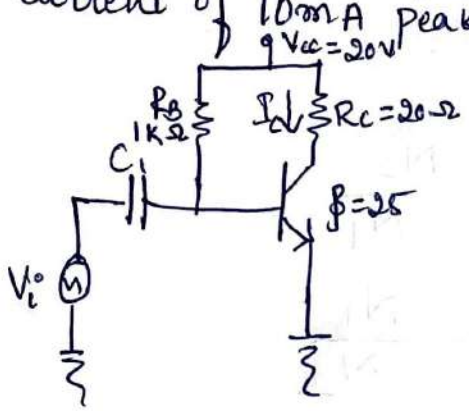
i/p dc power $\boxed{P_{i(dc)} = V_{cc} \cdot I_{CQ}}$

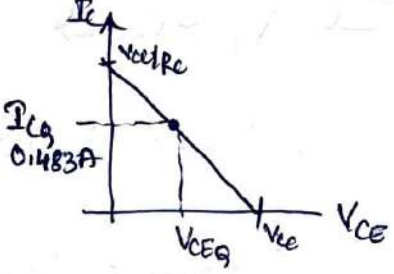
AC Analysis :-



Problem:-

① Calculate the i/p power, o/p power, and efficiency of the amplifier Circuit shown in figure for an i/p V.tg that results in a base Current of 10mA peak. $I_{CQ} = 0.483A$.





$P_i(dc) = V_{CC} \times I_{CQ}$

$= 20 \times 0.483$

$\boxed{P_i(dc) = 9.6\,W}$

$P_o(ac) = \frac{I_c^2(p) \cdot R_c}{2} = \frac{(250m)^2}{2} \times 20$

$\boxed{P_o(ac) = 0.625\,W}$

$I_C = \beta I_B$

$I_C = 25 \times 10m$

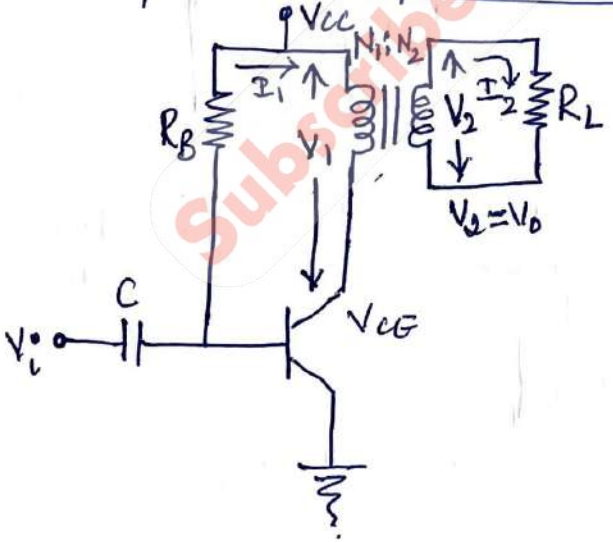
$\boxed{I_C = 250mA}$

$\%\eta = \frac{P_o(ac)}{P_i(dc)} \times 100\%$

$\%\eta = \frac{0.625}{9.6} \times 100\%$

$\boxed{\%\eta = 6.5\%}$

Transformer Coupled Class A Amplifier:



→ Instead of R_c a transformer is used to design a class A amplifier.

N_1 → no of turns in primary coil

N_2 → no of turns in secondary coil

V_1 → Voltage applied to primary

V_2 → Secondary Voltage

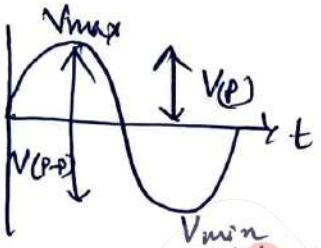
I_1 → Primary Current

I_2 → Secondary Current.

Expression for AC o/p power :-

Let
V_{im} → Peak value of primary V+q
I_{im} → peak value of primary current.

$$\therefore \boxed{P_{o(ac)} = \frac{V_{im} \cdot I_{im}}{2}} \rightarrow (1)$$



$$V_{im} = \frac{V_{(P-P)}}{2} \quad \& \quad I_{im} = \frac{I_{(P-P)}}{2}$$

$$V_p = V_m = \frac{V_{(P-P)}}{2}$$

$$\boxed{V_{im} = \frac{V_{max} - V_{min}}{2} \quad \& \quad I_{im} = \frac{I_{max} - I_{min}}{2}} \rightarrow (2)$$

$$V_{(P-P)} = V_{max} - V_{min}$$

$$V_{(P)} = V_m = \frac{(V_{max} - V_{min})}{2}$$

Put eqn (2) in (1)

$$P_{o(ac)} = \frac{1}{2} \cdot \left[\frac{V_{max} - V_{min}}{2} \cdot \frac{I_{max} - I_{min}}{2}\right]$$

$$\boxed{P_{oac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}}$$

Max efficiency :-

$V_{max} = 2V_{cc}$ $\quad V_{min} = 0$
$I_{max} = 2I_{CQ}$ $\quad I_{min} = 0$

$$P_{o(ac)} = \frac{(2V_{cc} - 0)(2I_{CQ} - 0)}{8}$$

$$P_{i(dc)} = V_{cc} \cdot I_{CQ}$$

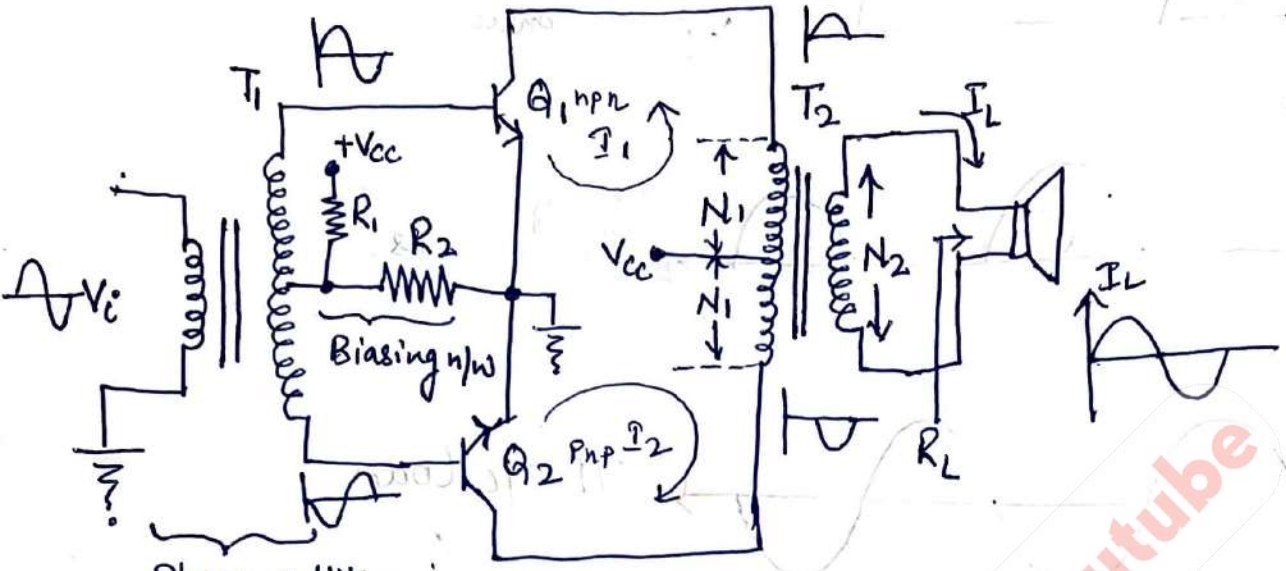
$$P_{o(ac)} = \frac{4 V_{cc} \cdot I_{CQ}}{8}$$

$$\boxed{P_{o(ac)} = \frac{V_{cc} \cdot I_{CQ}}{2}}$$

$$\% \eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\% = \frac{V_{cc} \cdot I_{CQ}}{2 V_{cc} \cdot I_{CQ}} \times 100\%$$

$$\boxed{\% \eta = 50\ \%}$$

Class-B Power Amplifier



T1 produces signal that is 180° out of phase

T2 Couples the o/p signal.

Class B push-pull amplifier

→ Class B produce 180° o/p hence two transistors are used to produce 360° o/p

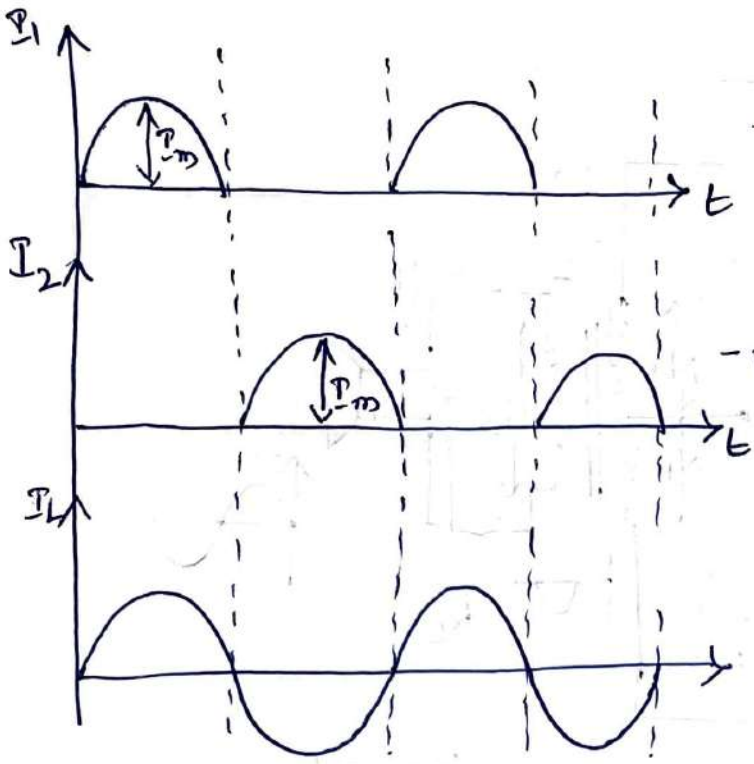
→ two transistors are different (npn & Pnp) to generate o/p in positive cycle and negative cycle (Complimentary transistors are used)

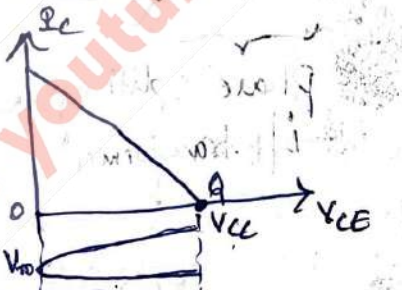
→ Both the transistors are biased at cutoff.

→ +ve half cycle Q_1 is ON & Q_2 is OFF we will get +ve half cycle at o/p

→ -ve half cycle Q_1 is OFF & Q_2 is ON. We will get -ve half cycle at o/p.

→ One transistor push the o/p to positive half and other transistor pull the o/p to negative half hence it is known as push-pull amplifier.





Power i/p

$$P_i(dc) = V_{cc} \times I_{dc}$$

$$I_{dc} = \frac{2I_m}{\pi} = I_{avg}$$

$$= \frac{2V_m}{\pi R_L}$$

$$I_m = \frac{V_m}{R_L}$$

∴ **Pow o/p** $P_i(dc) = \frac{2V_m V_{cc}}{\pi R_L}$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \qquad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$P_o(ac) = V_{rms} \cdot I_{rms}$$

$$P_o(ac) = \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$$

$$P_o(ac) = \frac{V_m \cdot I_m}{2} \Rightarrow P_o(ac) = \frac{V_m \cdot V_m}{2R_L} = \frac{V_m^2}{2R_L}$$

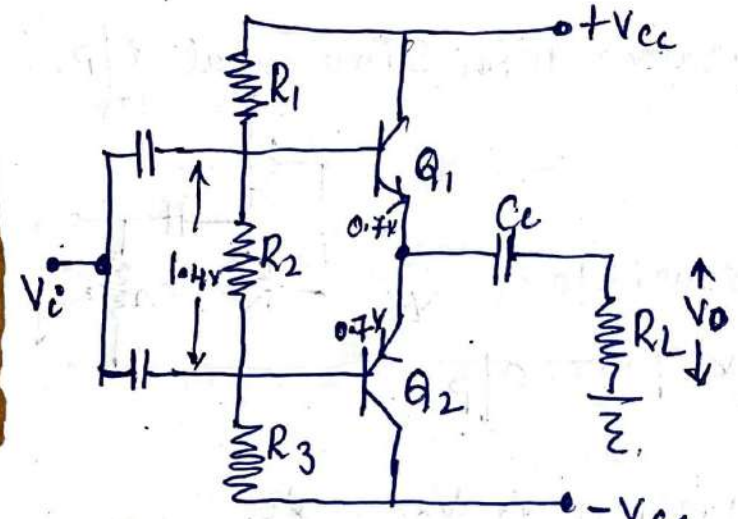
Efficiency :-

$$\%\eta = \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{V_m^2/2R_L}{2V_m V_{cc}/\pi R_L} \times 100\% \qquad \because V_m = V_{cc}$$

$$\%\eta = \frac{V_{cc}^2/2R_L}{2V_{cc}^2/\pi R_L} \times 100\% = \frac{\pi}{4} \times 100\%$$

$$\%\boxed{\eta = 78.5\%}$$

Class AB Power Amplifier.



(a) use of Vtg divider

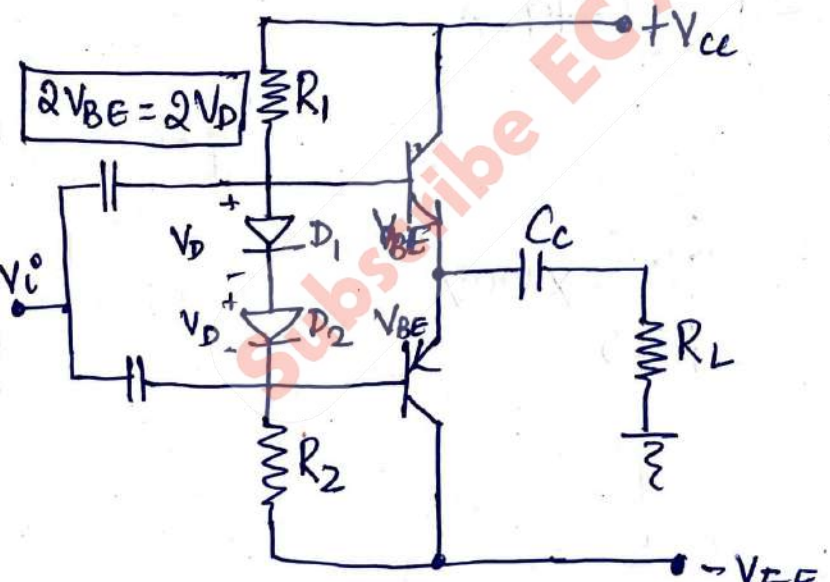
→ The base emitter junction of both Q_1 & Q_2 are required to provide a fixed bias.

→ Hence for silicon transister a fixed bias of $0.7+0.7=1.4V$ is required.

→ This can be achived by using Voltage divider circuit as shown in fig. (a).

→ This cut in vtg of 1.4V will change w.r.t temp. Hence there might be a possibility of distortion.

→ Solinsted of Resistor R_2 two diodes can be used. to provide fixed bias as shown in fig(b) below.



(b) use of pair of diodes

→ As temparature changes the diode characteristics get changed and maintain the necessary biasing required to overcome the distortion.

* Derivation for i/p power, o/p power & efficiency for class AB is same as class B amplifies *

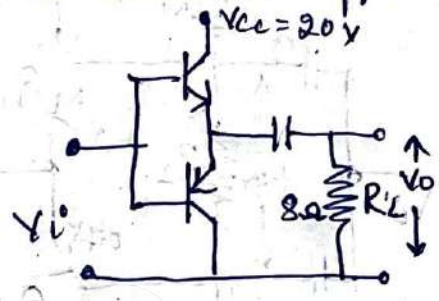
Problem :-

① The circuit shown in fig operates with sinusoidal i/p. Calculate

(i) Max Ac power o/p

(ii) Power dissipation in each transistor.

(iii) Conversion efficiency at max power o/p



Soln :- It is a single supply version $\therefore V_{cc} = \frac{20}{2} = 10\,V$

(i) $P_{o(ac)} = \frac{V_{cc}^2}{2R_L} = \frac{(10)^2}{2 \times 8} = 6.25\,W$

(ii) $P_{i(dc)} = V_{cc} \cdot I_{dc}$

$I_{dc} = \frac{2I_m}{\pi}$

$I_{dc} = \frac{2 \times 1.25}{\pi}$

$I_{dc} = 0.795\,A$

$I_m = \frac{V_m}{R_L} = \frac{V_{cc}}{R_L}$

$I_m = \frac{10}{8} = 1.25\,A$

$P_{i(dc)} = 10 \times 0.795$

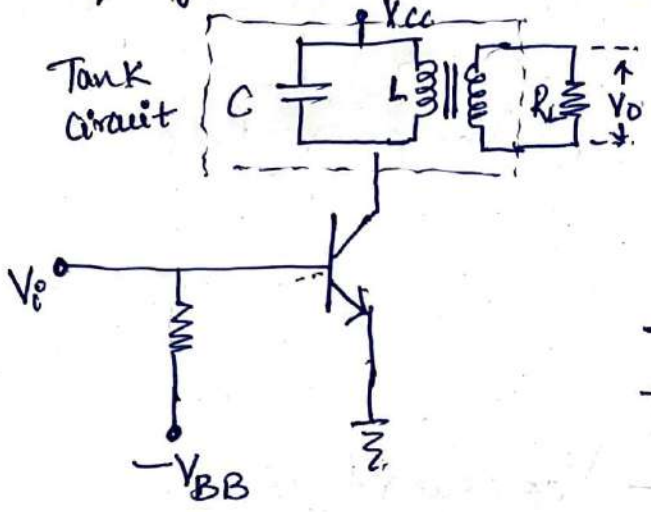
$P_{i(dc)} = 7.95\,W$

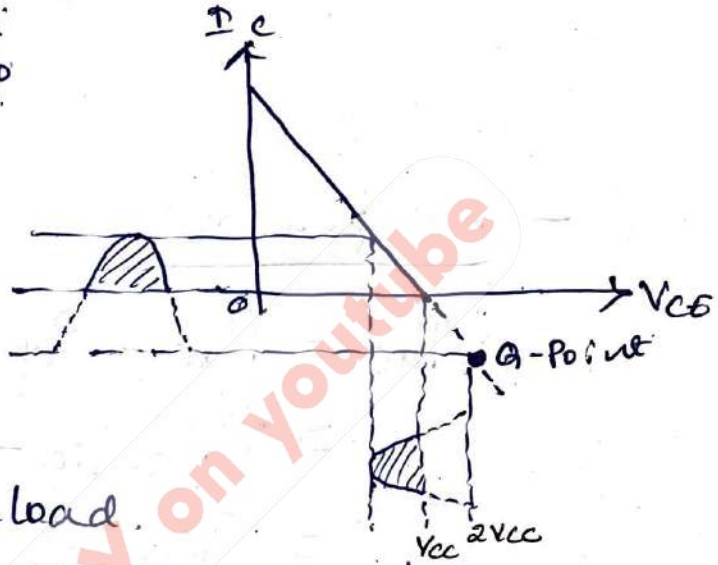
(iii) $\%\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\% = \frac{6.25}{7.95} \times 100\%$

$\%\eta = 78.6\%$

Class C Tuned Amplifier :-

→ Class C amplifier, transistor is 'ON' for less than half cycle (less than 180°) of the ac i/p signal.





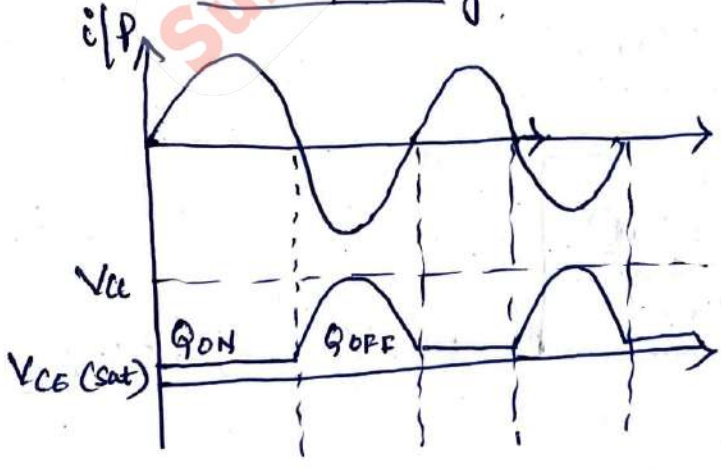
→ Tank ckt is used as a load.

→ For class C - operation, the transistor has a reverse biased B-E voltage at a Q-point.

→ $-V_{BB}$ is connected to the base circuit which reverse bias the B-E Junction.

→ The transistor will Conduct only when the input signal exceeds the Cut-in Vtg.

i/p & o/p Vtg :-



$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$V_{PP}(max) = 2V_{CC} + 0.7 + 0.7 = 2V_{CC} + 1.4$

$P_{dc} = \frac{V_{2rms}}{R_{dc}}$

- DC power

$P_{dc} = V_{cc} \cdot I_{dc}$

- Power dissipated by the transistor

$P_d = V_{CE(sat)} \cdot I_{dc}$.

- AC power

$$P_{ac} = P_{dc} - P_d$$
$$= V_{cc} \cdot I_{dc} - V_{CE(sat)} \cdot I_{dc}$$
$$= [V_{cc} - V_{CE(sat)}] I_{dc}$$

- Efficiency is given by,

$$\eta = \frac{P_{ac}}{P_{dc}}$$
$$= \frac{[V_{cc} - V_{CE(sat)}] I_{dc}}{V_{cc} \cdot I_{dc}}$$
$$\eta = \frac{V_{cc} - V_{CE(sat)}}{V_{cc}}$$

$$\boxed{\eta = 1 - \frac{V_{CE(sat)}}{V_{cc}}}$$

$\because V_{CE(sat)} \ll\ll V_{cc}$

$\therefore \boxed{\eta \geq 90\%}$

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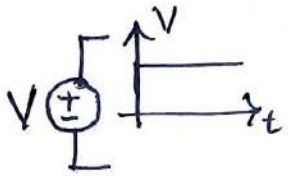
Module - 4

Opamp DC and AC Amplifiers

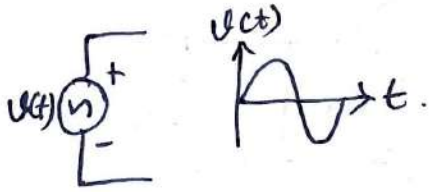
Module-4

→ In opamp i/p can be DC (or) AC

OPAMP ⇒ Operational AMPlifier.



DC supply



AC supply.

→ In opamp ~~two~~ 3 types of Circuit possible.

(i) Inverting amplifier.
(ii) Non Inverting amplifier.
(iii) differential amplifier.

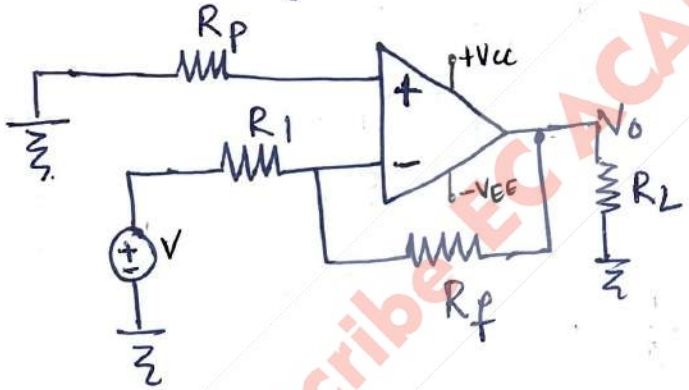
$$V_o = A(V_+ - V_-)$$

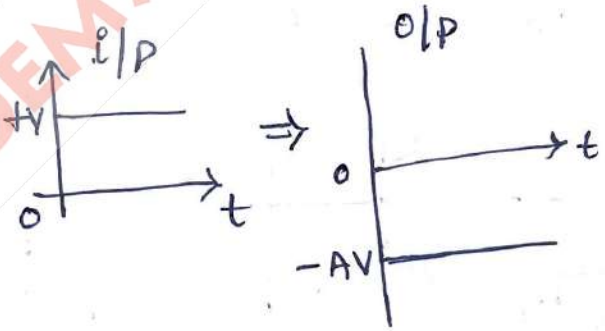
Inv. Amp. ⇒ $V_+ = 0$ ∴ $V_o = -AV_-$

non. Inv. Amp ⇒ $V_- = 0$ ∴ $V_o = AV_+$

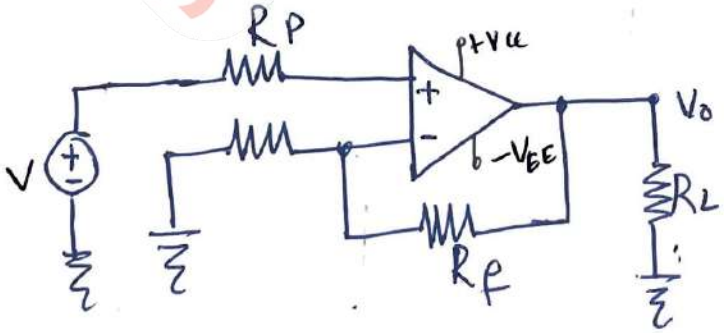
I. DC Input :- (DC signal Amplifier)

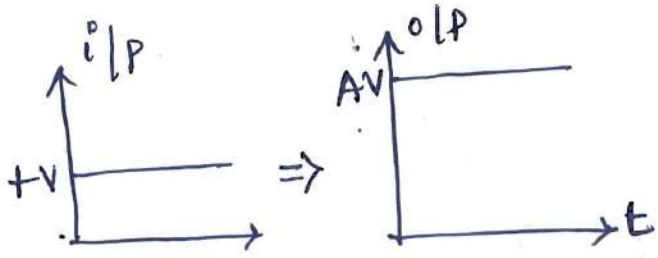
(i) Inverting Amplifier.



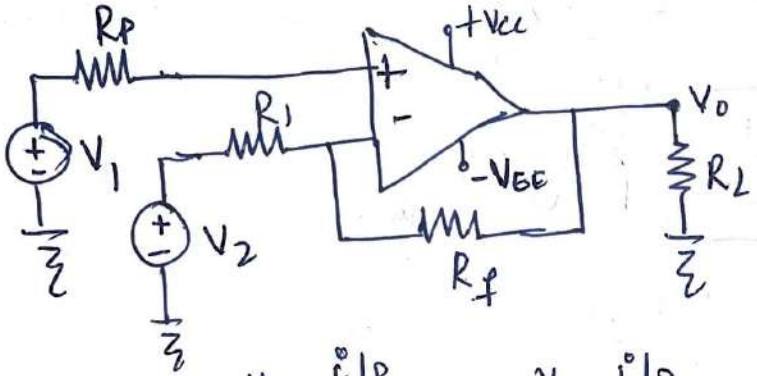


(ii) Non Inverting Amplifier

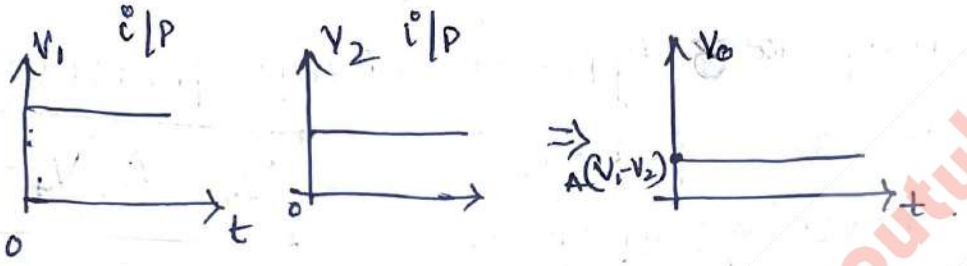




(iii) Differential Amplifier



$V_o = A(V_1 - V_2)$

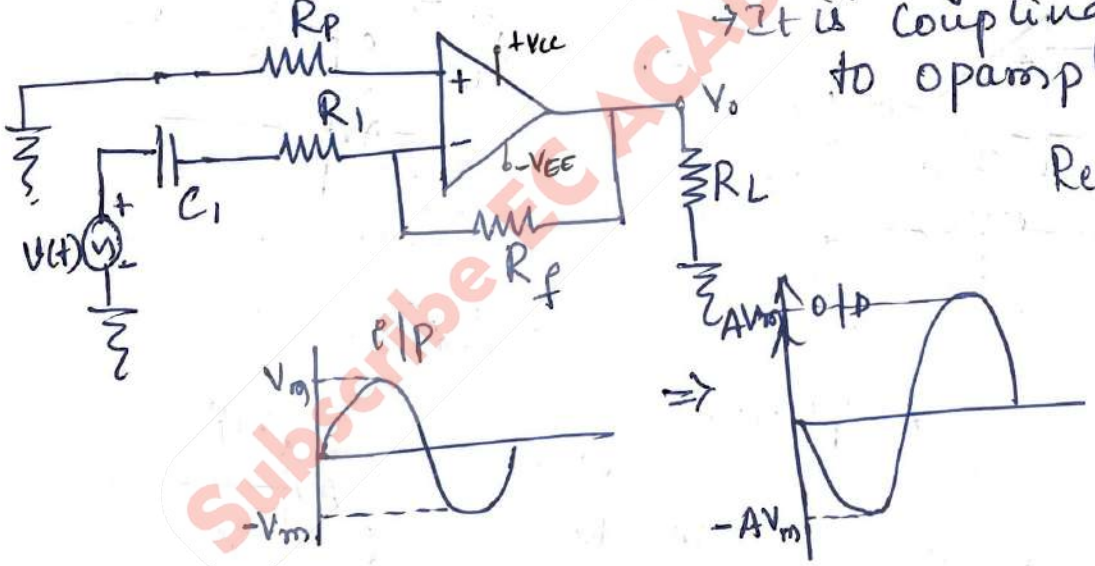


II AC. Input :- (AC Signal amplifier)

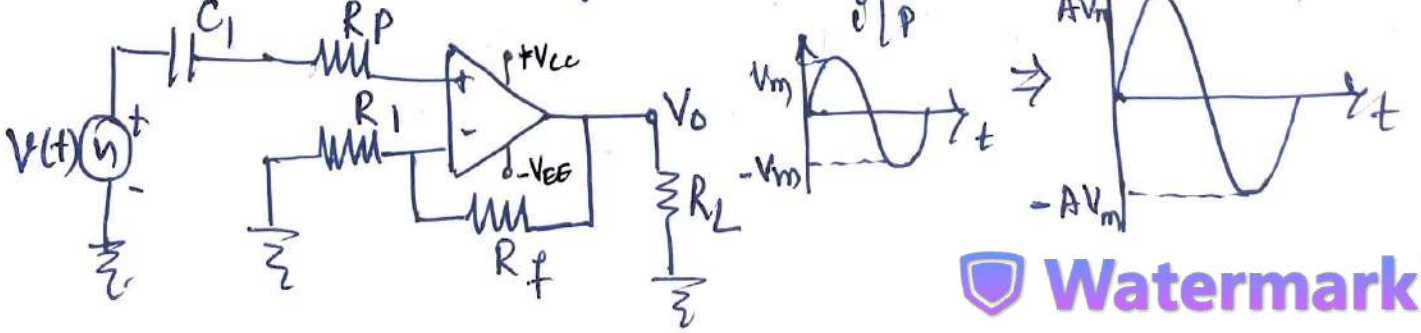
(i) Inverting Amplifier

$C_1 \rightarrow$ Coupling capacitor
$\rightarrow$ It is coupling the ac signal to opamp!

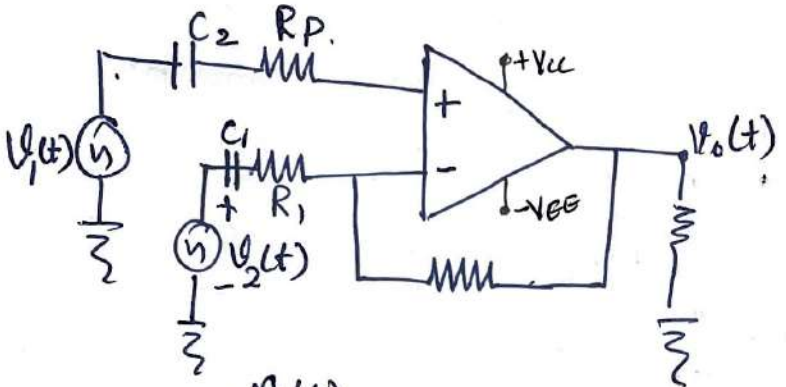
Reactance $X_{C_1} = R_1$



(ii) Non Inverting Amplifier

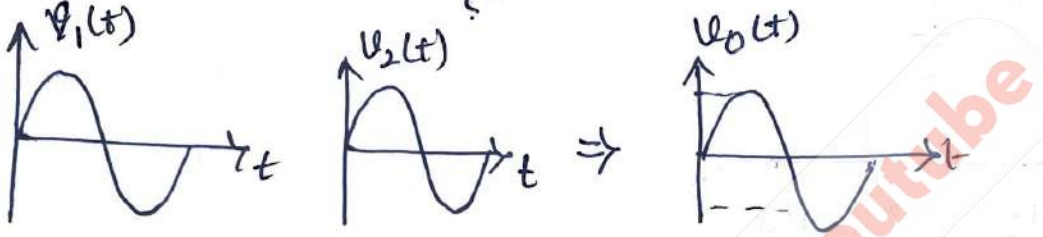


(iii) Differential Amplifier.



$V_o(t) = A(V_1(t) - V_2(t))$

$V_1 > V_2$ → Non Inverting o/p
$V_2 > V_1$ → Inverting o/p



DAC - Weighted Resistor :- (Data Converter)

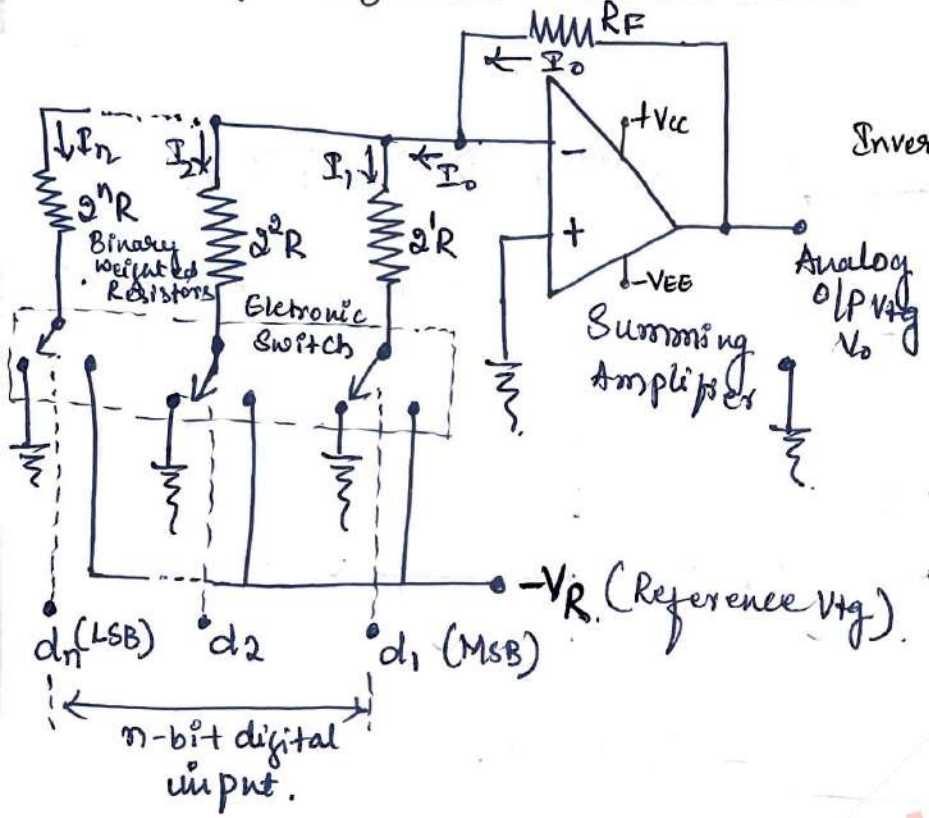
→ The signal is available in two forms
- (i) Digital signal → 0 & 1, more accurate, reliable & can provide security ⇒ Most widely used. but difficult to understand by user
- (ii) Analog signal → easily understand by the users.

→ At the user end the digital signal must be converted to analog signal, so that it can be easily understandable.

→ Two types of data converters.
- (i) Digital to analog converter (DAC)
- (ii) Analog to Digital Converter (ADC)

→ In DAC there are two types.
- (i) Binary weighted Resistor DAC
- (ii) R2R ladder DAC.

Binary weighted Resistor DAC :-



→ opamp is used in Inverting Summing Amplifier Configuration.

→ Binary weighted resistors have the values 2^1R, 2^2R ---- 2^nR.

→ Depending on number of bits the resistors are connected in the circuit.

→ the CKT is designed for n-bits binary no.

→ The switch is connected to the reference and to the reference Vtg.

→ For Ex:- For 3 bit DAC 3 resistors are connected in the circuit.

→ In the circuit if $d=0$ the switch is connected to ground and if $d=1$ then the switch is connected to the reference Vtg.

→ This is how the digital data is connected to the Circuit.

→ d_1 is considered as MSB & d_n is considered as LSB.

→ R_F = Feed back resistor & V_0 = O/P Vtg.

→ The O/P current is equal to current flowing through each resistor.

$$\therefore I_0 = I_1 d_1 + I_2 d_2 + I_3 d_3 \text{ ---} + I_n d_n$$

$$I_0 = \left[\frac{V_R d_1}{2R} + \frac{V_R d_2}{2^1R} + \frac{V_R d_3}{2^2R} \text{ ---} \frac{V_R}{2^nR} d_n\right]$$

$\therefore I_0 = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} \cdots + d_n 2^{-n}\right]$ ⑤

o/p vtg $V_0 = -I_0 R_F$.

$\therefore V_0 = -\frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right] R_F$.

Let $V_R = N_{FS}$ #[illegible]

$\rightarrow \frac{R_F}{R} = K$ if $R_F = R = 1$ then $K = 1$.

$\therefore \boxed{V_0 = -V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} \cdots + d_n 2^{-n}\right]}$

$d_1 \rightarrow$ MSB $\quad d_n \rightarrow$ LSB

→ o/p vtg is proportional to input digital data.

→ It is simple in design.

→ but it requires many number of resistors if no of bit required is more.

Prob:-

① For a 6 bit DAC for 111111 with $V_R = 10$ V. find V_0.

$V_0 = -V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} + d_5 2^{-5} + d_6 2^{-6}\right]$

$= -10\left[1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6}\right]$

$\boxed{V_0 = -9.844\text{V}}$

② For 5 bit DAC find V_0 for, $V_R = 10$x, Digital i/p = 10110 & Digital i/p = 10001

(i) $V_0 = -V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} + d_5 2^{-5}]$

$V_0 = -10 [1 \times 2^{-1} + 0 + 1 \times 2^{-3} + 1 \times 2^{-4} + 0]$

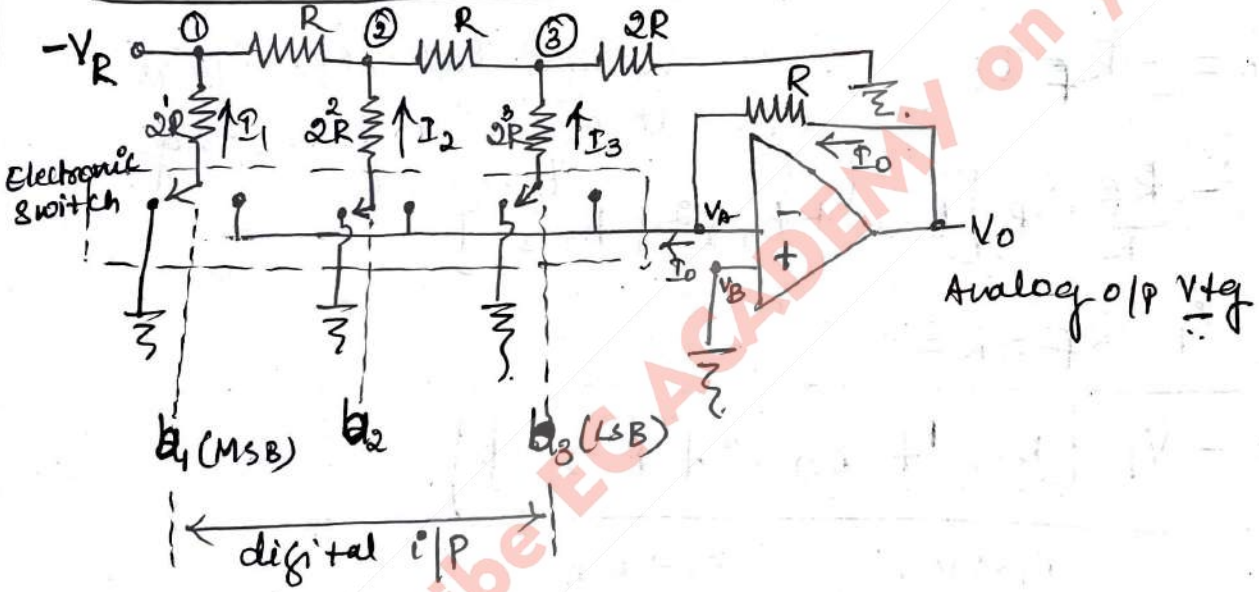
$\boxed{V_0 = -6.875V}$

(ii) $V_0 = -V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} + d_5 2^{-5}]$

$V_0 = -10 [1 \times 2^{-1} + 0 + 0 + 0 + 1 \times 2^{-5}]$

$\boxed{V_0 = 5.3125V}$

DAC - R2R ladder :- (Inverted R2R ladder)



→ Here two resistors R & 2R are used thats why it is known as R2R ladder DAC.

→ Three bit digital ~~source~~ data circuit is designed.

→ The switch is either connected to inverting terminal of an op amp (or) to the ground.

→ since the Vtg a/c non inverting terminal is zero

∴ $V_B = 0$ ∴ $V_A = 0$ due to virtual ground concept.

$I_1 = \frac{V_R}{2R} = \left(\frac{V_R}{R}\right)2^{-1}$ → node ①

$I_2 = \left(\frac{V_R}{2^2R}\right) = \left(\frac{V_R}{R}\right)2^{-2}$ → node ②

$I_3 = \left(\frac{V_R}{2^3R}\right) = \left(\frac{V_R}{R}\right)2^{-3}$ → node ③

$I_0 = b_1 I_1 + b_2 I_2 + b_3 I_3$

$= \left(\frac{V_R}{R}\right)2^{-1}b_1 + \left(\frac{V_R}{R}\right)2^{-2}b_2 + \left(\frac{V_R}{R}\right)2^{-3}b_3.$

$I_0 = \left(\frac{V_R}{R}\right)\left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}\right]$

$\because V_0 = -R_F I_0$ — -ve sign indicates i/p is connected to inverting terminal.

$V_0 = -\frac{R_f}{R} \cdot V_R \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}\right]$

if $R_F = R = 1$

$$\boxed{V_0 = -V_R\left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}\right]}$$

b_1 → MSB b_3 → LSB.

Successive Approximations - ADC (Converter)

→ ADC will be avilable in the form of IC's.

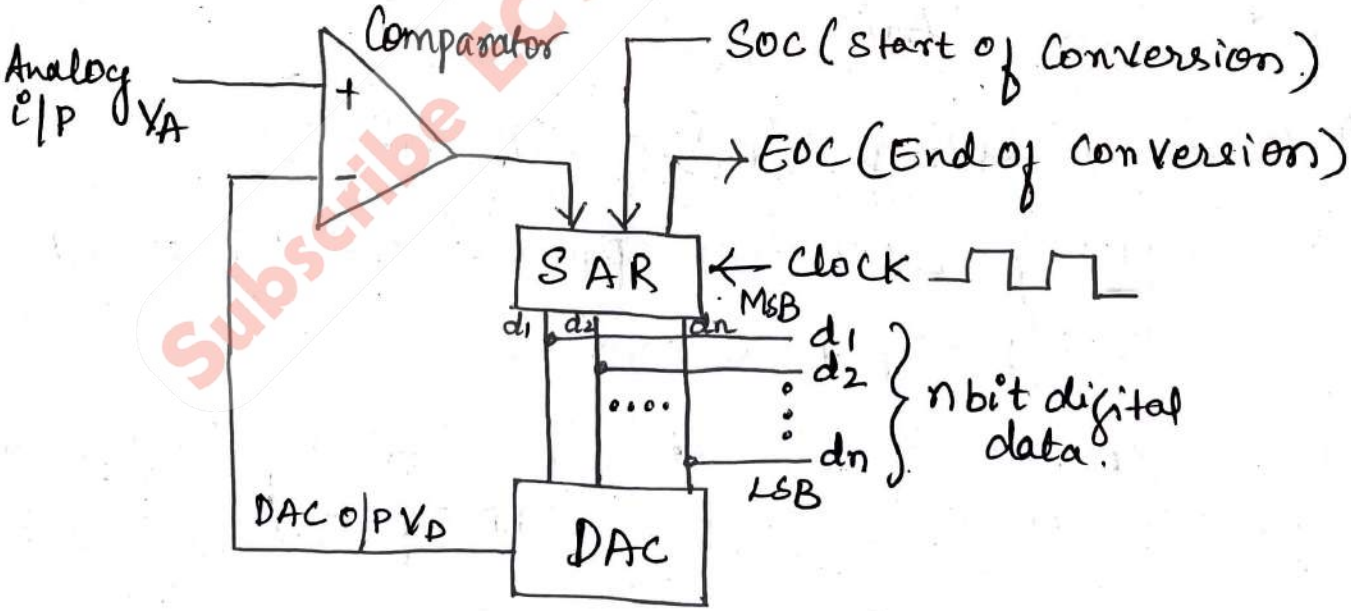
→ Most commonly used ADC is sucessive Approximations

→ Parameters to Consider while slecting an ADC includes, Resolution, Conversion time, Speed of Conversion, cost & no of bits.

→ Conversion time ⇒ is time taken by an ADC to Convert an Analog signal into digital form.

→ Ideally the Conversion time should be zero but practically. it should be as low as possible.

→ If Conversion time is faster then the speed of operation will be more.



→ SAR ⇒ Successive Approximation Resistor receives Comparator o/p, SOC signal & Clock signal as i/p and it provides EOC signal & digital o/p as o/p signal.

→ o/p of SAR is applied as i/p to DAC, the o/p of DAC is V_D is one of the i/p to the Comparator.

→ When V_D is less than V_A, then the Comparator o/p goes high

→ When V_D is greater than V_A, then the Comparator o/p goes low.

Operation:

→ Initially SOC is applied to SAR, then the SAR will reset.

→ then the o/p of SAR is $d_1 \text{---} d_8 = 0000\ 0000$ for 8-bit ADC.

→ Assume Analog i/p V+q $V_A = 11010010$.

→ Now o/p of SAR is applied as i/p to DAC, as the o/p of DAC is V_D.

→ Now V_D is less than V_A, the o/p of comparator goes high. = 1, then o/p of SAR will be

1000 0000

→ again This is applied as i/p to DAC. This V_D is less compared to V_A

→ The o/p of comparator goes high.

→ Then SAR o/p will be 1100 0000 (d_1 d_2)

→ This operation will repeat.

the o/p of SAR ⇒ 1110 0000

→ Now V_D is higher than V_A, the o/p of comparator goes low, then.

d_1 --- d_8 ⇒ 1101 0000

→ This process will continue until $V_D = V_A$.

→ Then SAR receives end of Conversion Command and stops the Conversion.
end EOC = 1

Ex:- ① For 8 bit SAR, f = 2MHz find the Conversion time for ADC.

Soln $f = 2MHz \Rightarrow T = \frac{1}{f} = \frac{1}{2M} \Rightarrow \boxed{T = 0.5\mu s}$

Conversion time = $n \times T = 8 \times 0.5\mu s$

$\boxed{\text{Conversion time} = 4\mu s.}$

② When i/p $V_{fg} = 10V$, for an 8 bit ADC find the resolution.

Soln :- The resolution can be defined as the max no of o/p bits available at the o/p of the ADC.

also, Resolution = $\frac{V_{FS}}{2^n - 1} = \frac{10}{2^8 - 1} = \frac{10}{255} \Rightarrow \boxed{R = 0.39V}$

$V_A = 13.2\,V \Rightarrow 1101$

Successive Approximation

Example (1)

	SAR Present State	V_0	SAR Next State	
SOC=1	0 0 0 0 $V_A > V_D$	1	1 0 0 0	
	1 0 0 0	1	1 1 0 0	
	1 1 0 0	1	1 1 1 0	
	1 1 1 0	0	1 1 0 1	$\Rightarrow V_A = V_D$ then EOC=1
			13 V	

Example (2).

V_A = $2^7\ 2^6\ 2^5\ 2^4\ 2^3\ 2^2\ 2^1\ 2^0$
1 1 0 1 0 1 0 0 ⇒ 212V
128 64 16 4

Initially SAR is reset 0000 0000
Comp o/p = 1
$V_A > V_D$ ^ Then MSB bit is set as 1

$d_1 \text{---} d_8$ ⇒ 1000 0000

again $V_A > V_D$ Comp o/p = 1

$d_1 \text{---} d_8$ ⇒ 1100 0000

$V_A > V_D$ Comp o/p = 1

$d_1 \text{---} d_8$ ⇒ 1110 0000

$V_A < V_D$ Comp o/p = 0

$d_1 \text{---} d_8$ ⇒ 1101 0000

↑ Previous set bit is reset & next bit is set.

$V_A > V_D$ Comp o/p = 1

$d_1 \text{---} d_8$ ⇒ 1101 1000

$V_A < V_D$ Comp o/p = 0

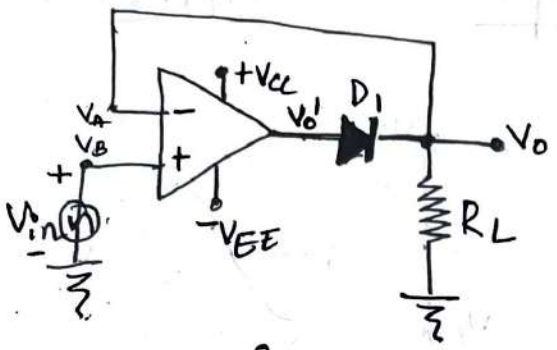
$d_1 \text{---} d_8$ ⇒ 1101 0100 ⇒ $V_A = V_D$

$V_A < V_D$ Comp o/p = 0 o/p EOC = 1

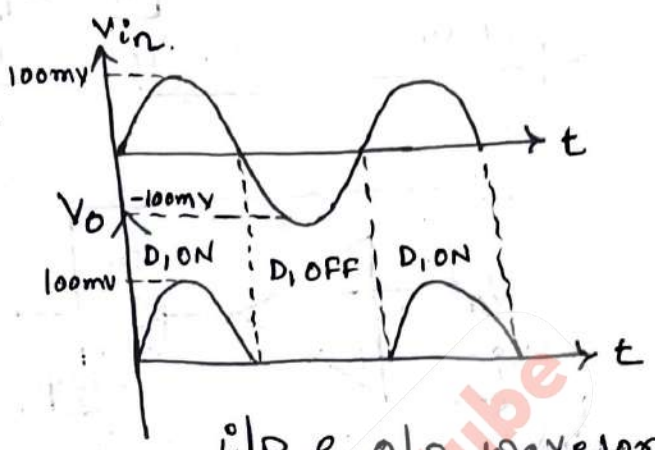
$d_1 \text{---} d_8$ ⇒ 1101 0010 ⇒ $V_A = V_D$ then EOC = 1

Small signal Half wave rectifier:

(i) Positive - Small Signal Half wave rectifier



Circuit



i/p & o/p waveforms

Precisely

→ are used to rectify voltages having amplitude less than 0.7V

→ Hence the name - Small Signal precision rectifier.

During

→ Positive half cycle of i/p → opamp produces high positive o/p (V_o')

→ hence Diode D_1 is forward biased hence o/p is obtained at load resistor.

→ The circuit is similar to Voltage follower Circuit

Hence,

due to Virtual ground

$V_A = V_B$ ∵ $V_B = V_{in}$ ∴ $V_A = V_{in}$.

∵ $\boxed{V_o = V_A}$ ∴ $\boxed{V_o = V_{in}}$

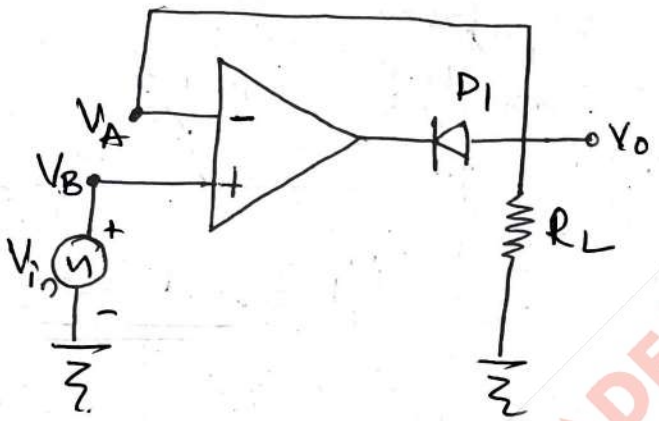
→ During negative half cycle of i/p

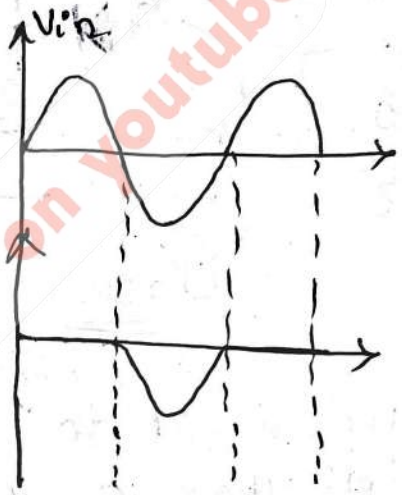
$\boxed{V_o' = -V_{in}}$

→ Hence diode will be reverse biased and hence there will be no o/p Vtg.

$V_o = 0$

(ii) Negative Small Signal Half Wave rectifier:





→ During positive half of i/p cycle diode D_1 is reverse biased & hence no o/p Vtg

$V_o = 0$

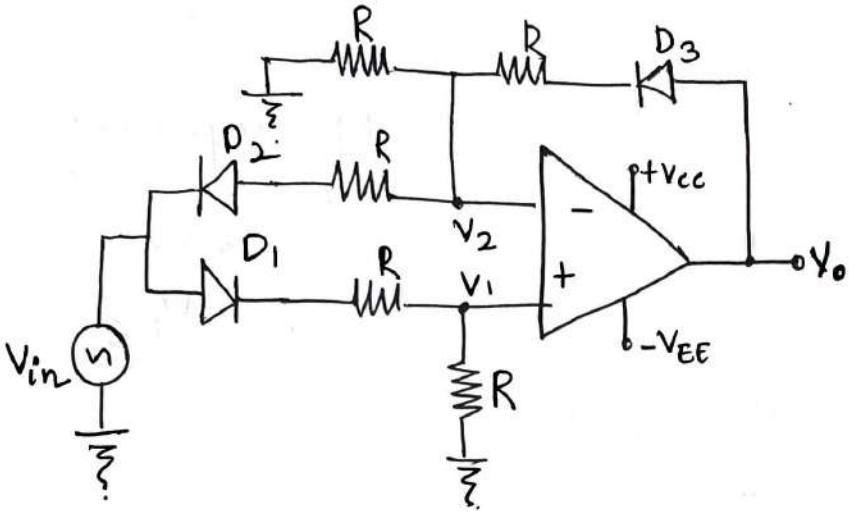
→ During negative half of i/p cycle diode D_1 is forward biased hence o/p is obtained accross the load resistor.

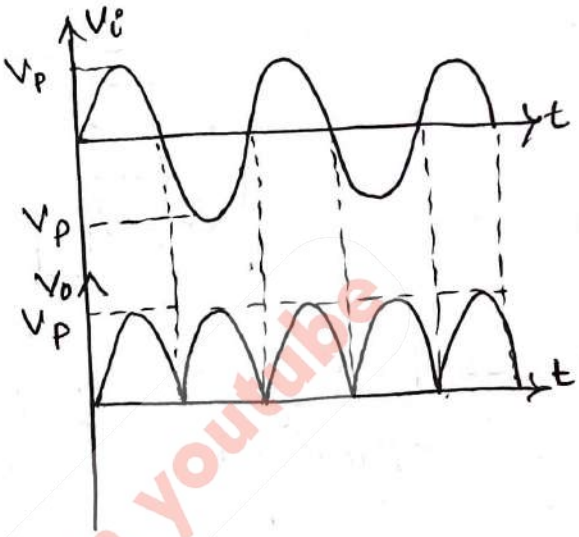
$V_A = V_B$ ∵ $V_B = -V_{in}$ ∴ $V_A = -V_{in}$

∵ $V_o = V_A \Rightarrow$ $V_o = -V_{in}$

Absolute Value output Circuit

→ This circuit produce the o/p signal in Positive direction, hence it is also called as full wave rectifier

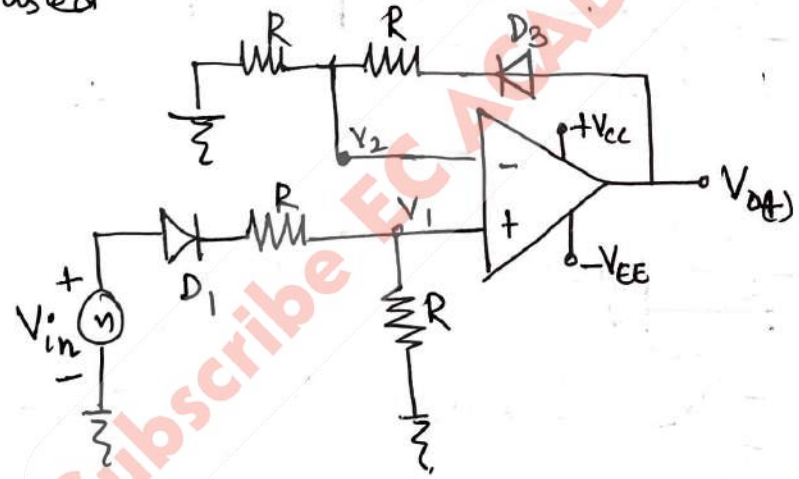




Working :-

→ During positive half of i/p cycle.

→ D_1 will be Forward biased and D_2 will be reverse biased



→ In this Condition. V_1 will be (at non-Inverting termina

$$V_1 = \frac{R(V_p - V_{D1})}{R+R}$$

V_p → Peak Vtg of i/p.

V_{D1} → Vtg drop across Diode D_1

→ ~~The Vtg~~ $V_1 = \frac{R(V_p - V_{D1})}{2R}$

$$\boxed{V_1 = \frac{(V_p - V_{D1})}{2}}$$

$$V_2 = \frac{R(V_O - V_{D3})}{R+R} = \frac{R(V_{O(+)} - V_{D3})}{2R} \Rightarrow \boxed{V_2 = \frac{V_{O(+)} - V_{D3}}{2}}$$ (16)

From Virtual ground $V_1 = V_2$

$$\therefore \frac{V_P - V_{D1}}{2} = \frac{V_{O(+)} - V_{D3}}{2}$$

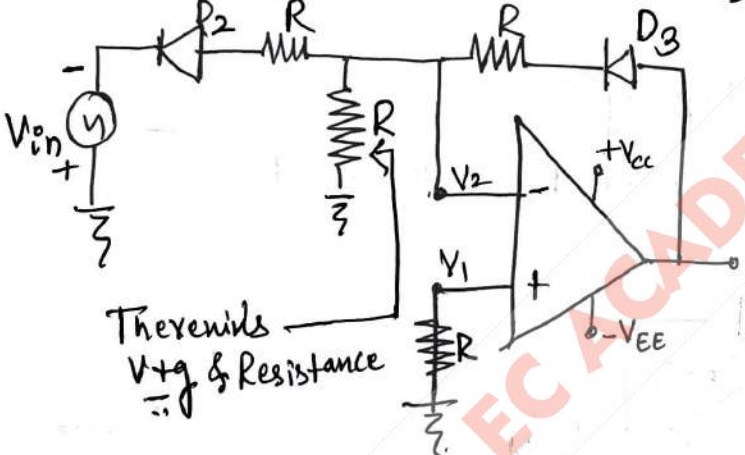
$\because$ V+g drop across both the diodes are same

$\therefore V_{D1} = V_{D3}$

$$\boxed{V_{O(+)} = V_P}$$

→ During negative half of i/p cycle.

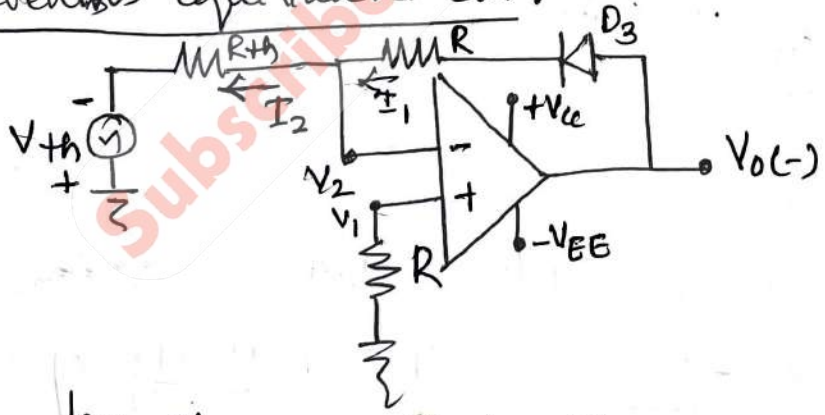
→ Diode D_2 will be Forward biased and D_1 will be Reverse biased



$$V_{th} = R\left(\frac{V_P - V_{D2}}{R+R}\right) \Rightarrow \boxed{V_{th} = \frac{V_P - V_{D2}}{2}}$$

$$R_{th} = \frac{R^2}{2R} \Rightarrow \boxed{R_{th} = \frac{R}{2}}$$

Thevenin's equivalent CKt:-



$$\Downarrow$$

$$V_{O(-)} - V_{D3} = V_P - V_{D2}$$

$\because V_{D3} = V_{D2}$

$$\boxed{V_{O(-)} = V_P}$$

by Chr of diode $I_1 = I_2$

$$\frac{(V_{O(-)} - V_{D3}) - V_2}{R} = \frac{V_2 - V_{th}}{R/2}$$

From Virtual ground $V_1 = V_2$ $\because V_1 = 0$ $\therefore V_2 = 0$

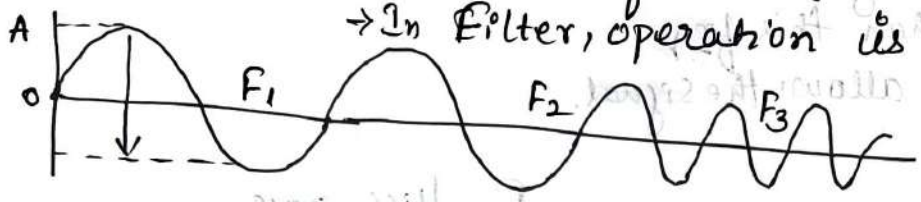
$$V_{O(-)} - V_{D3} = -2V_{th}$$

$$\Downarrow$$

Filters :-

Ex:- Water Filter → Pure water (selective part)
→ Block unwanted particles.

Filter :- It is the circuit that pass the selective portions and ~~Pass~~ Block the unwanted portion of the signal.



→ In Filter, operation is related to Frequency

→ If we want to pass a particular Frequency (F_1) and block other frequency (F_2 & F_3). This type of operation can be performed in Filters.

→ So a particular frq is passed & other frequencies are blocked in Filters

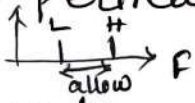
Filters
- → Passive Filters ⇒ R, L & C are used (without amplifier)
- → Active Filters ⇒ along with R, L & C we are using Opamp. (with amplifier)

4 types of operations

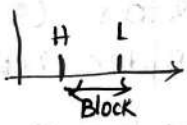
a) Low pass Filters → which pass low frequencies & block high frequencies.

b) High pass Filter → which pass high frequencies.

c) Band pass Filters → which Can pass particular frequencies.



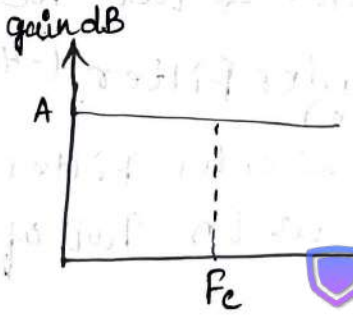
d) Band Reject Filter → It Blocks particular frequies and allows all other frequencies



(1) Low pass Filters :-

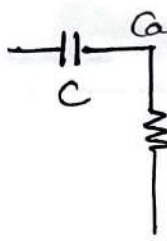
F_c → Cutoff frq

low ⇒ less than F_c.
high ⇒ more than F_c



⇒

PB → Pass Band
SB → Stop Band.

→ 

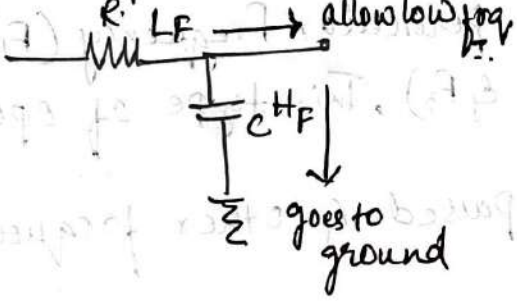
⇒ allow – High frq
block – low frq

$$F = \frac{1}{2\pi RC}$$

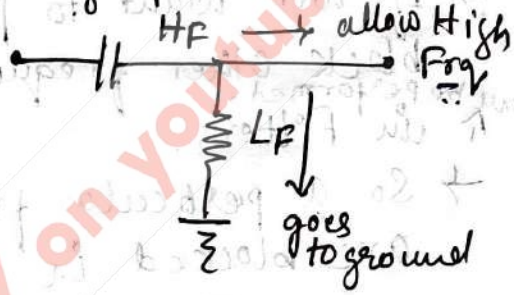
– Capacitor & Resistor values will decide what frq is to allow & block.

– Below this frq Capacitor block the signal
– Greater than this frq capacitor allows the signal.

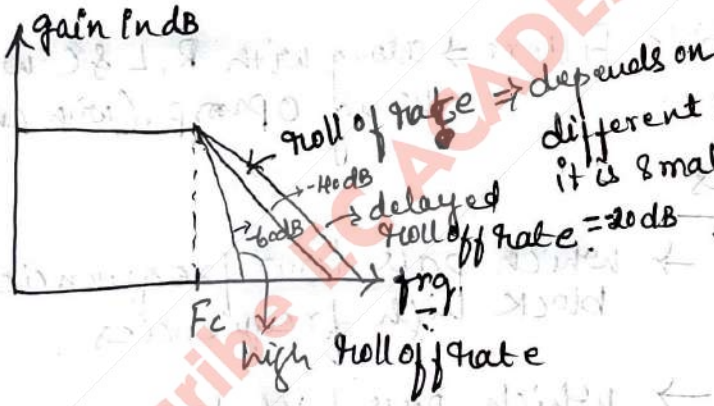
→ For low pass.

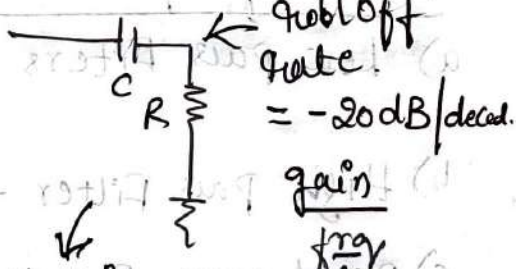


For High pass.



Actual response :-





Same circuit connected in series. then roll off rate will be = -40 dB/dec.

– If One capacitor & One resistor is present
⇒ First order Filter (single pole) (-20 dB/dec roll off rate)

– If two Capacitor & two resistor is present
⇒ Second order Filter (double pole) (-40 dB/dec roll off rate)

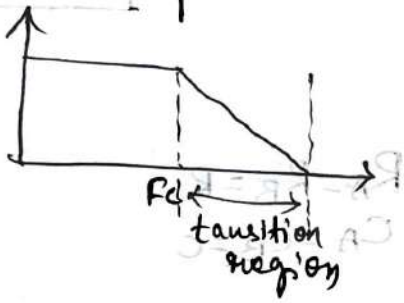
Both Fist & second order Filter operation is same only difference is in roll off rate.

Pass Band :-

- is the range of frequencies that are allowed to pass through the Filter with min attenuation.
- Frequencies less than F_c will be passed

Transition region :-

- change b/w one pass band to Stop band.



Stop band :-

- The particular range of frq that have most attenuation.
- Frq greater than F_c

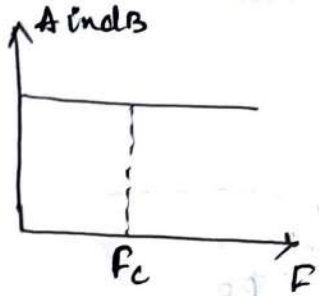
Cut Off frq :- (Critical Frq)

- It is the Isolation b/w Pass band and Stop band.

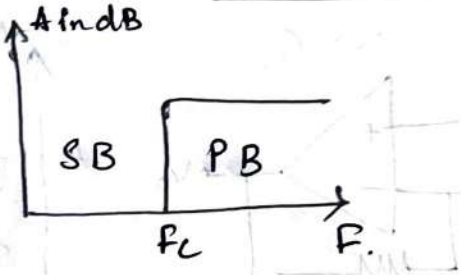
$$F_c = \frac{1}{2\pi RC}$$

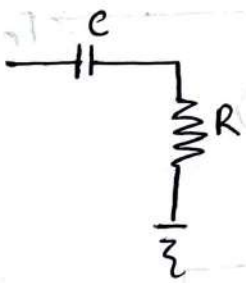
Band width :- Range from 0 to $F_c = F_c$.

High Pass Filter

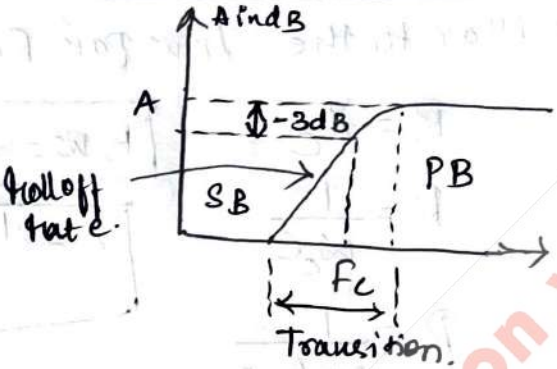


Ideal response.





Actual response



(1) **Pass Band** :- The frqy greater than F_c will pass & frqy less than F_c will be attenuated.

(2) **Stop Band** :- The frqy less than F_c.

(3) **Transition region** :-

Roll off rate = -20 dB/dec ⇒ First order filter
= -40 dB/dec ⇒ Second order filter

$$F_c = \frac{1}{2\pi RC}$$

$$A = 1 + \frac{R_f}{R_1}$$

Active Filters

(i) Low pass Filter

(ii) High pass Filter.

Filters ⇒ Frequency selective circuit

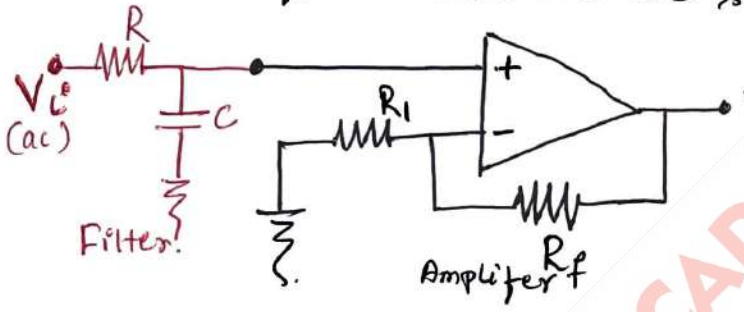
- Active Filter (Active components) Opamp, transistors etc. $V_{out} > V_{in}$ (Filter operation & amplification)
- Passive Filter (Passive components) Inductor, Capacitor Resistor. $V_{out} < V_{in}$ (Only Filter operation)

(i) Low pass :- pass low freq (ii) High pass :- pass high freq

I. Low pass Filter :- a. First order

→ uses non Inverting Amplifier

→ i/p should be ac signal (freq present in only ac)



Filter design :-

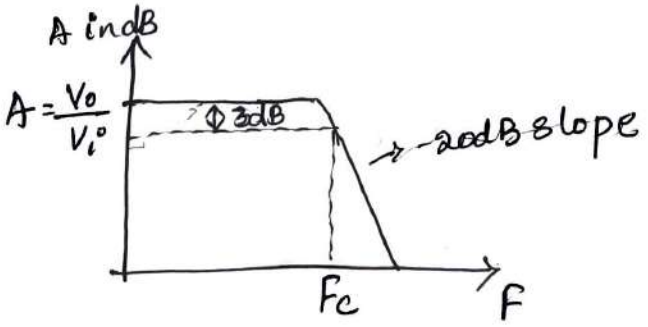
Cutoff freq $F_c = \frac{1}{2\pi RC}$ here $R = X_C$ X_C → Capacitance reactance

$R = \frac{1}{\omega_c C}$

$R = \frac{1}{2\pi F_c C}$

Band width 0 to f_c ∴ $BW = F_c - 0$

$BW = F_c$



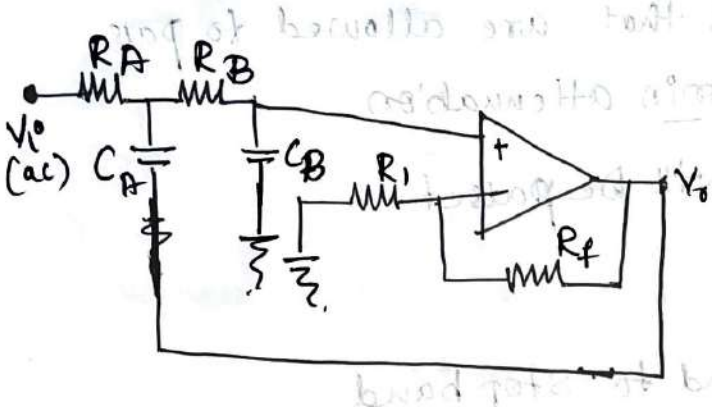
Amplifier design :-

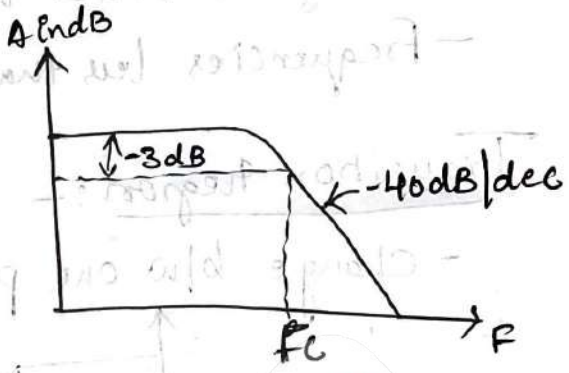
$A = 1 + \frac{R_f}{R_1}$

b. Second order

Second order LPF

- Also known as two pole selective circuit.





Design :-

$$F_c = \frac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$$

if $R_A = R_B = R$, $C_A = C_B = C$

$$= \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$\boxed{F_c = \frac{1}{2\pi RC}}$$

- we have same fromulas for F_c, BW & A as in Firstorder.
- only difference is in Roll off rate = -40 dB/dec for 2nd order.
- Slope of 2nd order is Very less compared to first order filter

Bandwidth $= F_c$

gain $A = 1 + \frac{R_f}{R_1}$

Butterworth Filter :-

- Filter with gain $A = 1.56$.

Problem ① :- Design a Butterworth lowpass Filter with $F_c = 7.23$ k. Assume equal R & C. $C = 22$ nF & $R_2 = 1\text{k}\Omega$ → R_f

Soln:-

$$F_c = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi F_c C} = \frac{1}{2\pi \times 7.2\times10^{3} \times 22\times10^{-9}} \Rightarrow \boxed{R = 1\text{k}\Omega}$$

$R_A = R_B = 1\text{K}\Omega$

take $\boxed{A = 1.56}$

$A = 1 + \frac{R_f}{R_1}$

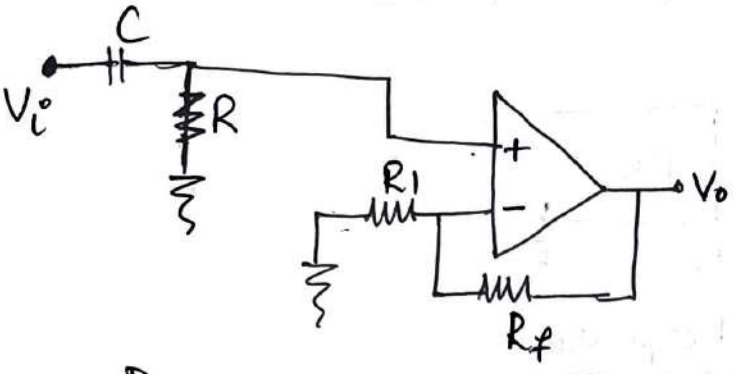
For Butterworth Filter $A = 1.56$

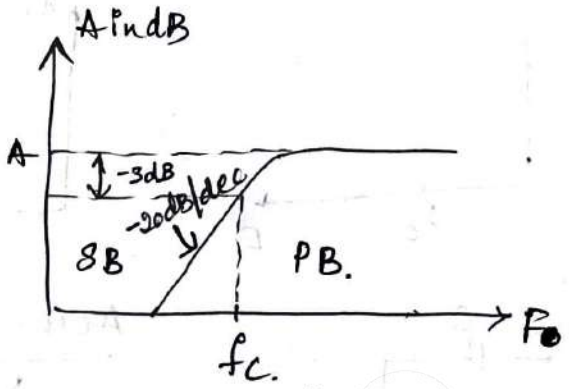
$1.56 = 1 + \frac{1\text{K}}{R_1} \Rightarrow \frac{1\text{K}}{R_1} = 0.56 \Rightarrow \boxed{R_1 = 1.78\text{K}\Omega}$

* Draw the Ckt & Substitute all the values.

II. High pass filter:

(a) First order HPF:-





Design:- (similar to the Low pass filter).

$$F_c = \frac{1}{2\pi R_c}$$

$$R = X_c$$

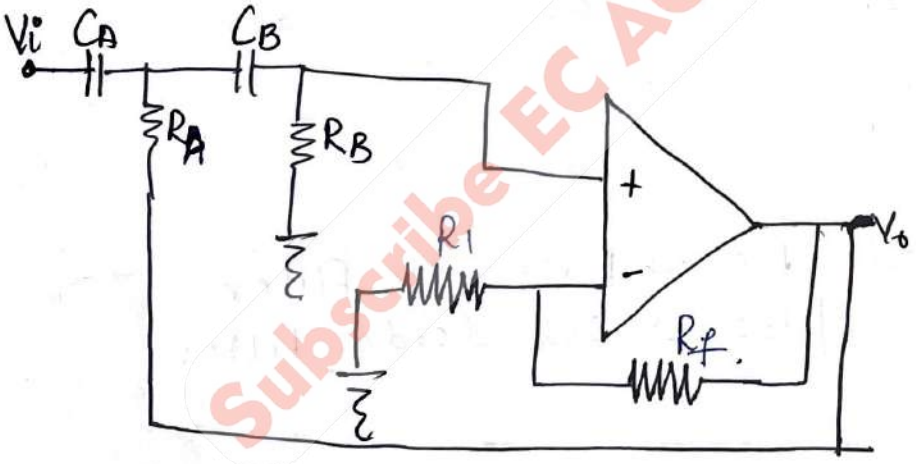
$$R = \frac{1}{\omega_c C}$$

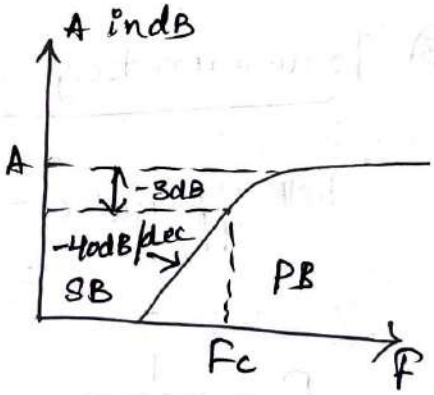
$$R = \frac{1}{2\pi f_c C}.$$

$$BW = F_c$$

$$A = 1 + \frac{R_f}{R_1}$$

(b) Second order HPF:-





Design:-

$$F_c = \frac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$$

if $R_A = R_B = R$

$C_A = C_B = C$

$$F_c = \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$F_c = \frac{1}{2\pi RC}$$

$$BW = F_c$$

$$A = 1 + \frac{R_f}{R_1}$$

Butter worth Filter:

- Filter with gain

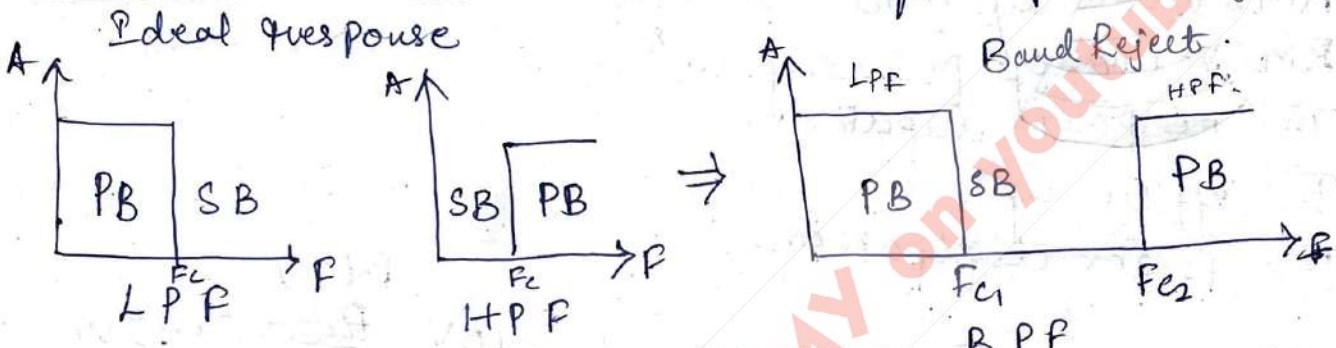
$$A = 1.56$$

- We have discussed 5 types of Filters.

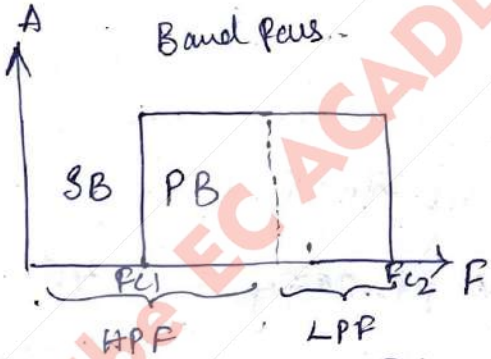
(i) First order Low pass Filter
(ii) First order High pass Filter
(iii) Second order Low pass Filter
(iv) Second order Highpass Filter

} all these filters design using (V) Butterworth Filter.

Band pass Filters :- Combination of low pass & High pass Filter



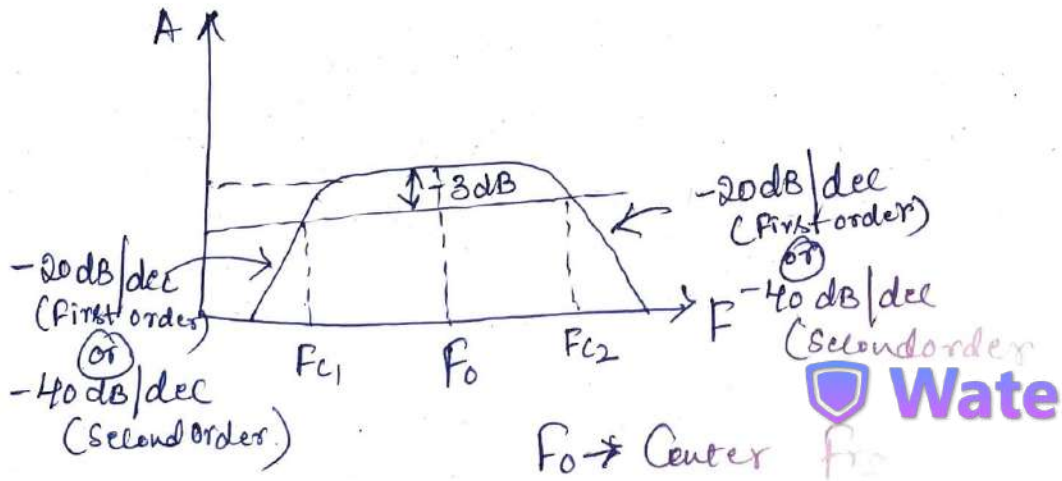
- It is known as Band reject Filter.
- (or) Band stop Filter



- Band pass Filter

- In Band pass Filter

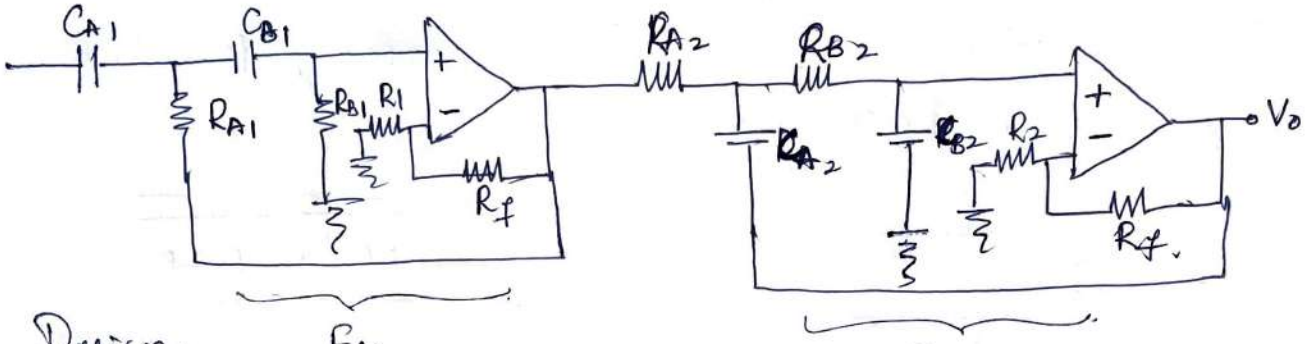
Actual response.



Fo → Center fr

Band Pass Filter

i/p — HPF — LPF — o/p

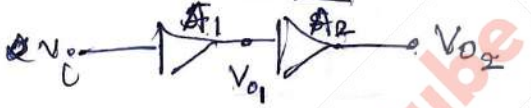


Design :-

$$F_{c1} = \frac{1}{2\pi\sqrt{R_{A1}R_{B1}C_{A1}C_{B1}}}$$

$$F_{c2} = \frac{1}{2\pi\sqrt{R_{A2}R_{B2}C_{A2}C_{B2}}}$$

Series Amplifier



$$V_{o2} = A_2 V_{o1}$$

$$\boxed{V_{o2} = A_2 A_1 V_i}$$

$\therefore$ gain

$$A = \left(1 + \frac{R_f}{R_1}\right)\left(1 + \frac{R_f}{R_2}\right)$$

Bandwidth :-

$$\boxed{BW = F_{c2} - F_{c1}}$$

Center freq $\Rightarrow$ $\boxed{F_0 = \sqrt{F_{c1} F_{c2}}}$

Quality factor $Q = \dfrac{\text{Center freq}}{BW} = \dfrac{F_0}{F_{c2} - F_{c1}}$

↓ represents Constant gain portion.

$$\boxed{Q = \frac{\sqrt{F_{c1} F_{c2}}}{F_{c2} - F_{c1}}}$$

– to get good Quality factor we should have good Center freq.

Problem :-

(1) In a BPF ; $R_{A1} = R_{B1} = 33K$ & $R_{A2} = R_{B2} = 10K$, $C_{A1} = C_{A2} = C_{B1} = C_{B2} = 100PF$, Find Quality Factor ; Bandwidth & Center freq.

$$Q = \frac{\sqrt{F_{C1} F_2}}{F_{C2} - F_{C1}}$$

(05)

$$Q = \frac{f_o}{B.W.}$$

$$F_{C1} = \frac{1}{2\pi\sqrt{R_{A1} R_{B1} C_{A1} C_{B1}}}$$

$$= \frac{1}{2\pi RC} = \frac{1}{2\pi \times 33K \times 100P}$$

$$\boxed{F_{C1} = 48.23KHz}$$

$$F_{C2} = \frac{1}{2\pi\sqrt{R_{A2} R_{B2} C_{A2} C_{B2}}}$$

$$f_{C2} = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi \times 10K \times 100P}$$

$$\boxed{F_{C2} = 159.15KHz}$$

$$BW = F_{C2} - F_{C1} = 159.15K - 48.23K$$

$$\boxed{BW = 110.93KHz}$$

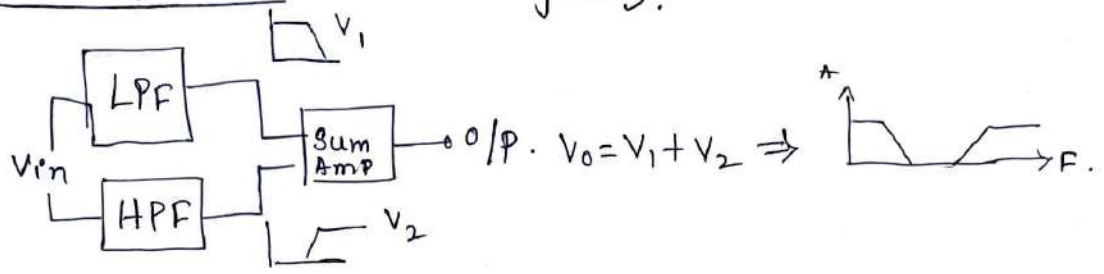
$$F_o = \sqrt{F_1 F_{C2}} = \sqrt{48.23K \times 159.15K}$$

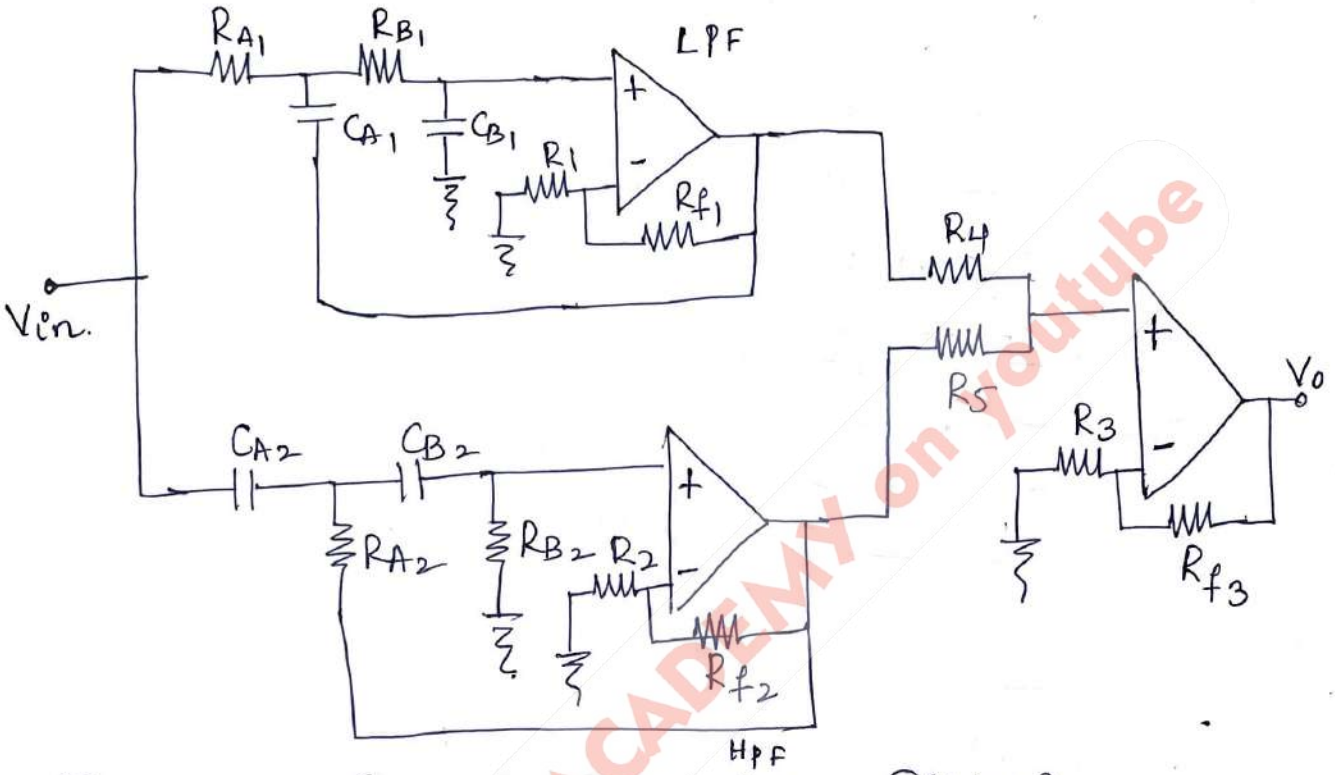
$$F_o = 87.611 \times 10^3$$

$$Q = \frac{F_o}{BW} = \frac{87.611K}{110.93K} = \underline{0.79}$$

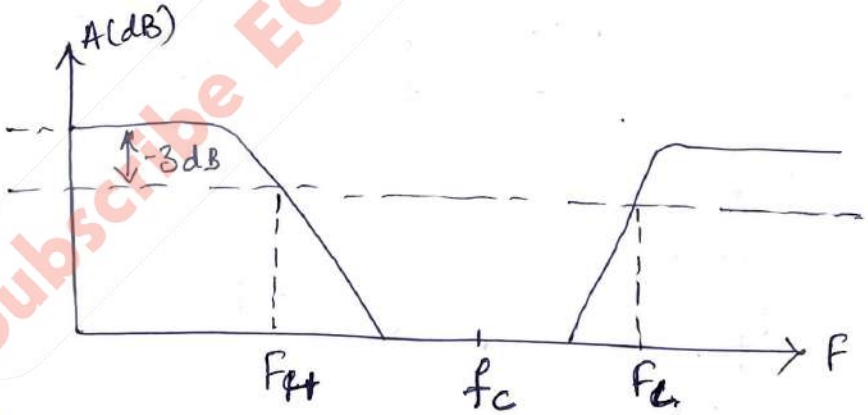
$$\boxed{Q = 0.79}$$

Band stop Filter (Band Reject).





Design :- (Same as Band pass Filter)



$$f_c = \sqrt{F_H F_L}$$

$$F_H = \frac{1}{2\pi\sqrt{R_{A1}R_{B1}C_{A1}C_{B1}}} = \frac{1}{2\pi RC} \quad \text{if } R_{A1}=R_{B1}=R,\ C_{A1}=C_{B1}=C$$

$$F_L = \frac{1}{2\pi\sqrt{R_{A2}R_{B2}C_{A2}C_{B2}}} = \frac{1}{2\pi R'C'} \quad \text{if } R_{A2}=R_B=R',\ C_{A1}=C_{B1}=C'$$

Problem :- Design a Band rejected filter having $F_H = 400\ Hz$ & $F_L = 2KHz$ with ~~band~~ pass band gain of 2.

Ans:- given, $F_H = 400\ Hz$ & $F_L = 2KHz$.

assume $C = 0.01\mu F = C_{A2} = C_{B2}$

- For high pass section.

$$F_L = \frac{1}{2\pi R'C'} \Rightarrow 2K = \frac{1}{2\pi R' \times 0.01\mu} \Rightarrow R' = 7.957K\Omega$$

$= R_{A2} = R_{B2}$

- For low pass section → assume $C = 0.05\mu F = C_{A1} = C_{B1}$

$$F_H = \frac{1}{2\pi RC} \Rightarrow 400 = \frac{1}{2\pi R \times 0.05\mu} \Rightarrow R = 7.957K\Omega$$

$\simeq R_{A1} = R_{B1}$

- gain of both sections must be 2.

$$\therefore A_F = 1 + \frac{R_f}{R_1} = 2.$$

$$\frac{R_f}{R_1} = 1$$

$$R_f = R_1 = 10K\Omega \text{ (assume)}.$$

- For Summing Amplifier. let gain be = 1

$$R_4 = R_5 = R_{f3} = 10K\Omega.$$

$$R_3 = \frac{R}{3} = \frac{10K}{3} = 3.33K\Omega.$$

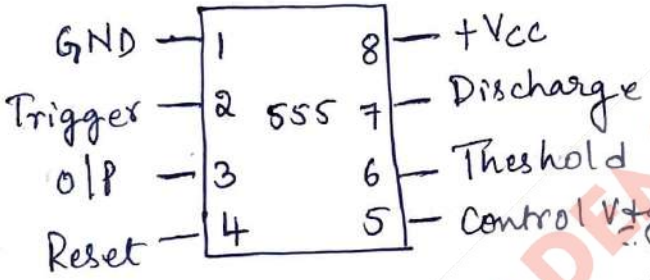
* Write the Circuit *

555 Timer IC

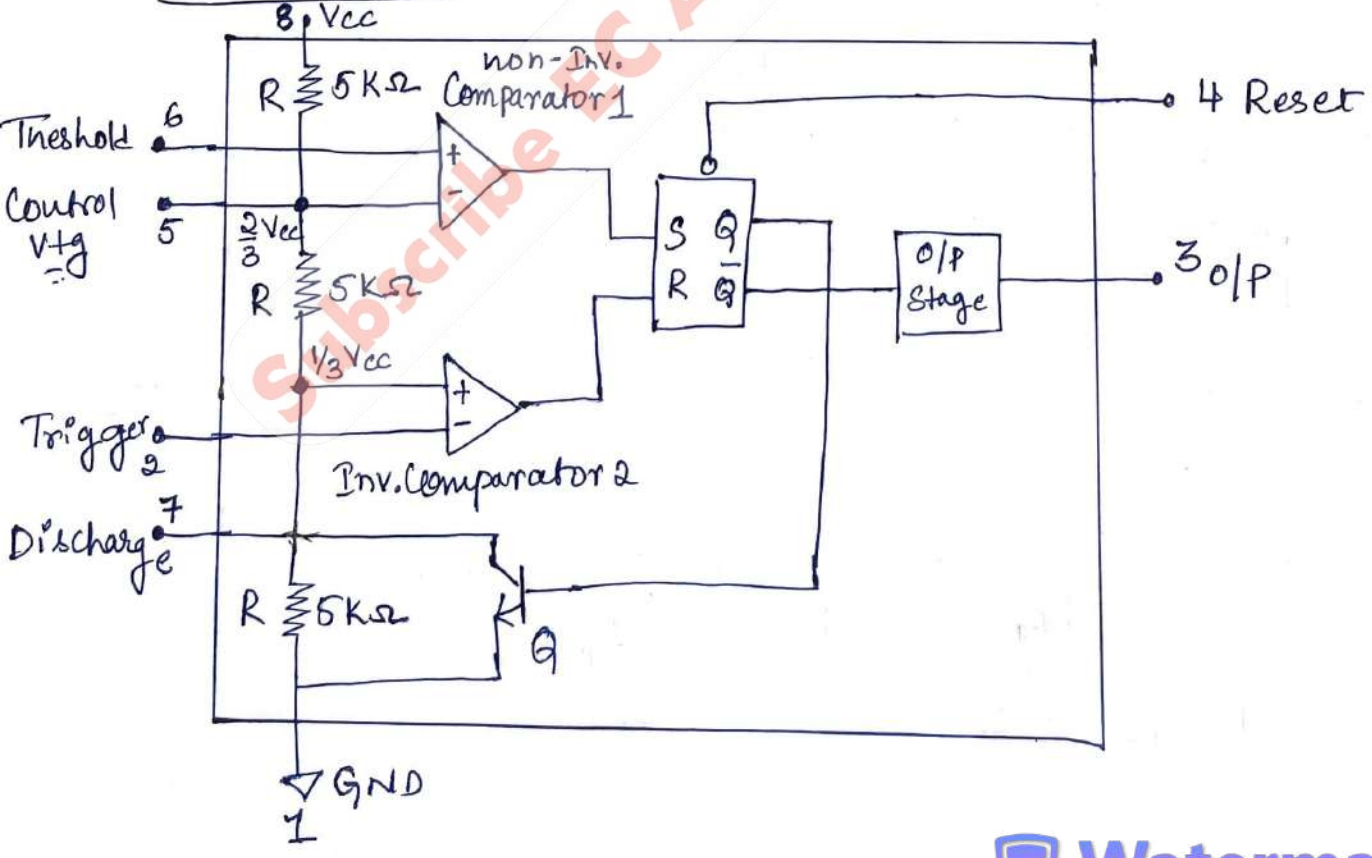
- It can produce accurate & highly stable time delays (or) Oscillations.

- It is a 8-pin IC
- 3 resistors are used with 5KΩ hence 555 timer

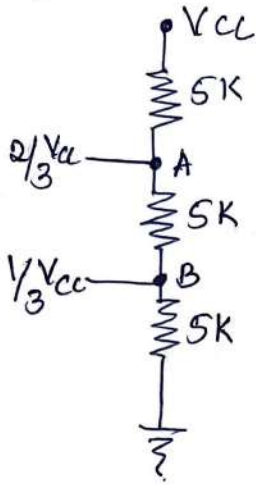
Applications – Monostable, astable multivibrator
- Waveform generator.
- DC to DC Converters
- Voltage regulator
- Alarms



Block diagram :-



1. Resistors

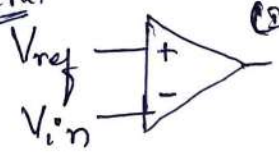


$$V_A = \frac{10}{15} V_{cc} \Rightarrow \boxed{V_A = 2/3\, V_{cc}}$$

$$V_B = \frac{5}{15} V_{cc} \Rightarrow \boxed{V_B = 1/3\, V_{cc}}$$

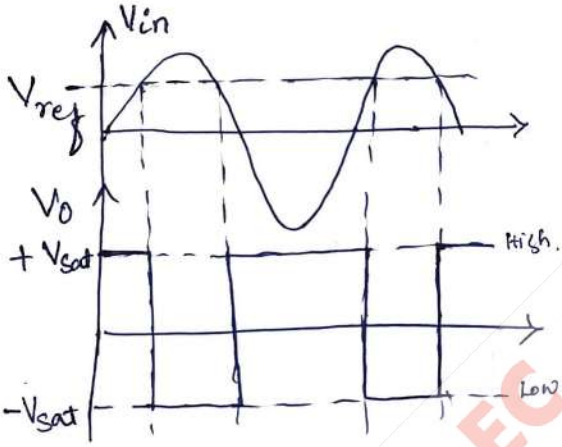
2. Comparator.

General



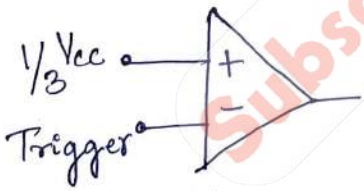
(Inverted comparator)
∵ i/p is given to -ve terminal.

- Since it is open loop OPAMP
  o/p ⇒ +Vsat (or) -Vsat.



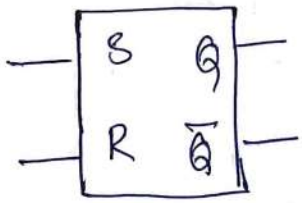
If $V_{in} > V_{ref} \Rightarrow V_o = -V_{sat}$.
$V_{in} < V_{ref} \Rightarrow V_o = +V_{sat}$.

As per diagram.



Trg > 1/3 Vcc ⇒ o/p = LOW
Trg < 1/3 Vcc ⇒ o/p = HIGH

3. Flipflop



S	R	Q o/p	Q̄
0	0	No change	NC
0	1	Reset	Set
1	0	Set	Reset
1	1	Invalid.	Invalid

→ At Trigger pin i/p is applied to Inverting Comparator

→ if negative pulse is applied to pin 2

then $V_{in} < V_{ref}$

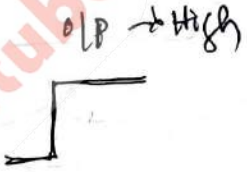
– o/p of Comparator will be high (1)

→ high o/p of Comparator is given as i/p at 'R' of SR Flip Flop.

then $Q = 0$

$\bar{Q} = 1$

– o/p of 555 timer is high.



→ Q is connected as i/p to the transistor then transistor will be off.

→ At non-inverting amplifier

when $V_{th} > 2/3 V_{cc}$

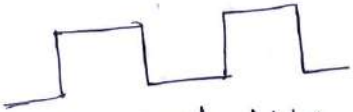
– o/p of comp will be high.

– high o/p of comp is given as i/p at 'S' of SR Flip Flop

then $Q = 1$

$\bar{Q} = 0$

– o/p of 555 timer is low

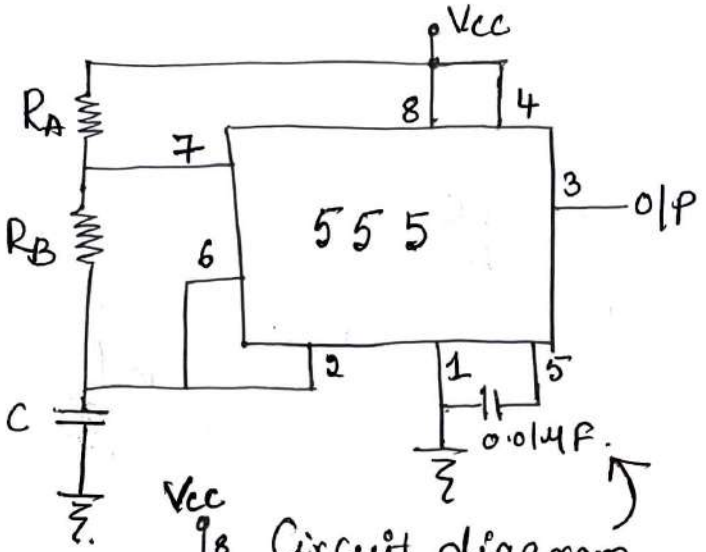


– Purpose of Control Vtg is to change the pulse width with the help of POT.

– Discharge pin is used to discharge any charges using external circuit.

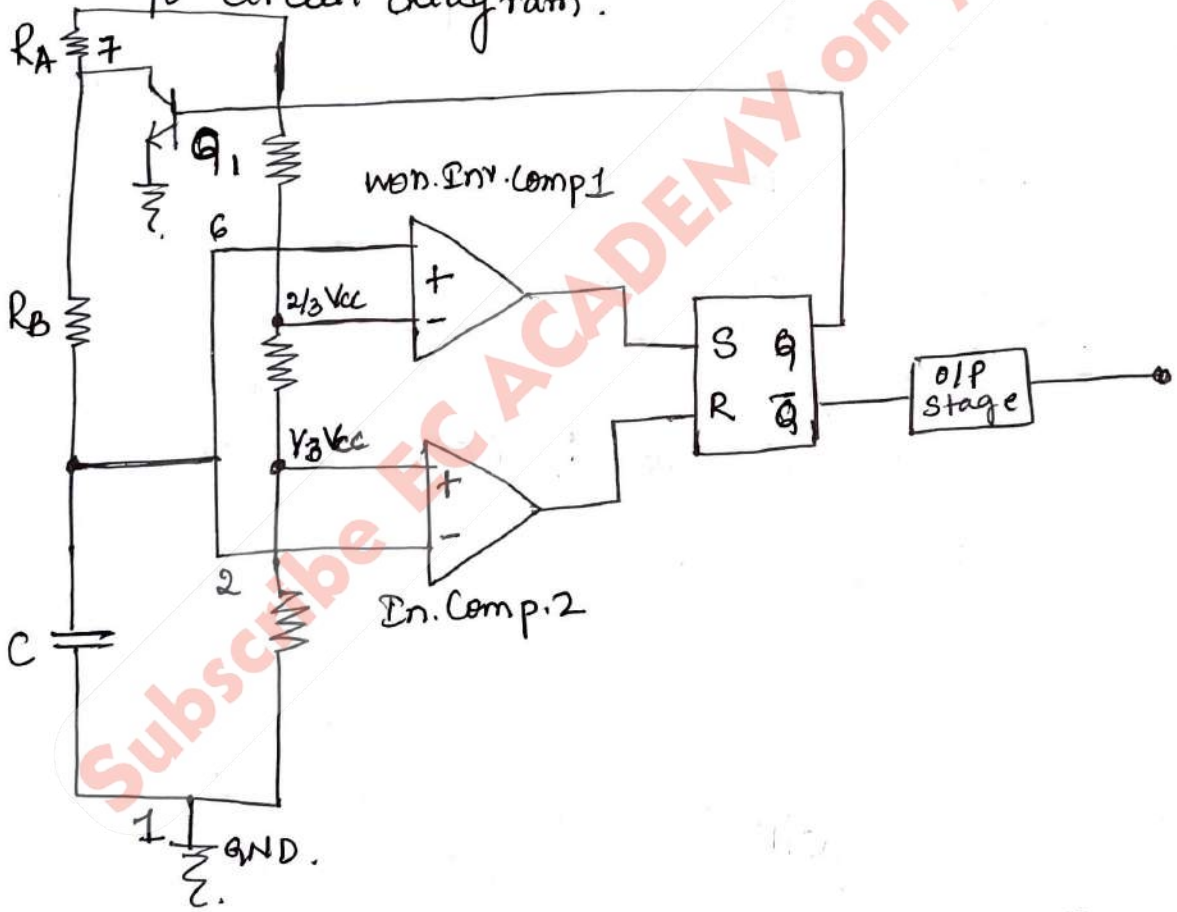
Astable Multivibrator :- [555 timer]

- Free running
- does not require external trigger



- R_A, R_B & C → will drive the circuit.
- And helps in free running.

Circuit diagram.



- Pin 6 is threshold which is i/p to non Inverting Comparator 1
- Pin 2 is trigger which is i/p to Inverting Comparator 2

- Q is connected to transistor base
- $\bar{Q}$ is connected to the o/p stage. → 1 will appear at o/p
- Let us assume $\bar{Q} = 1$ & $Q = 0$. since Q is connected to base of transistor Q_1
- transistor will be in cutoff.
- Hence Capacitor will charge through R_A & R_B.
- Now Vcc will appear as i/p to comp 1

  then $V_{c\bullet} > 2/3 V_{cc}$ ∴ o/p of comp 1 = 1

  hence. S = 1 ∴ Q = 1 & $\bar{Q} = 0$.

- Therefore **o/p = 0**
- $V_{c\bullet}$ will also appear as i/p to comp 2.

  ∵ It is inverting comparator ∴ $V_{c\bullet} > 2/3 V_{cc}$.

  o/p of comp 1 = 0

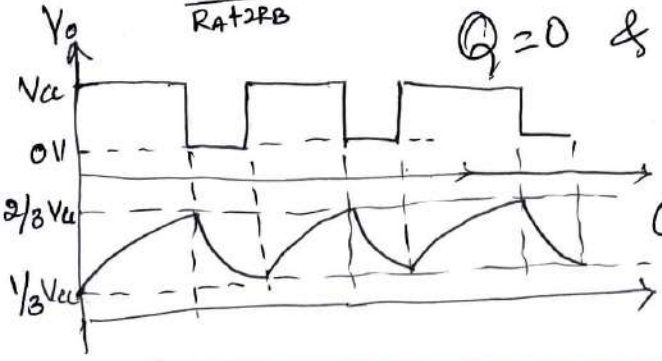
- Since Q = 1 ∴ transistor Q_1 is on.
- Capacitor will discharge., hence V_c will be less.
- Now when V_c is i/p to comp 2

  $V_c < 1/3 V_{cc}$ then comp 2 o/p = 1

  Q = 0 & $\bar{Q} = 1$ ∴ **o/p sage = 1**

⑤ Duty cycle = $\frac{t_c}{T} \times 100$

$= \frac{R_A + R_B}{R_A + 2R_B} \times 100$



① Charging time = $t_c = 0.69 (R_A + R_B) C$

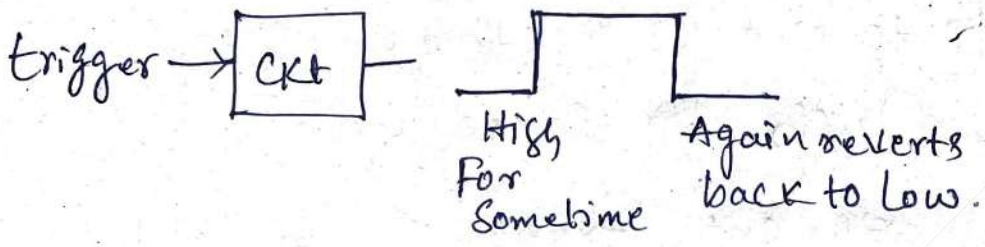
② discharging time = $t_d = 0.69 (R_B) C$

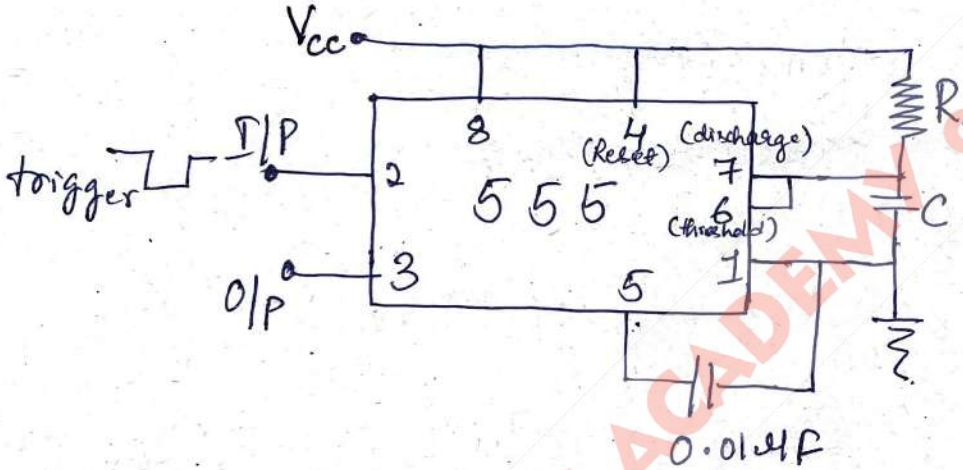
Capacitor time period = $T = t_c + t_d = 0.69 (R_A + 2R_B) C$

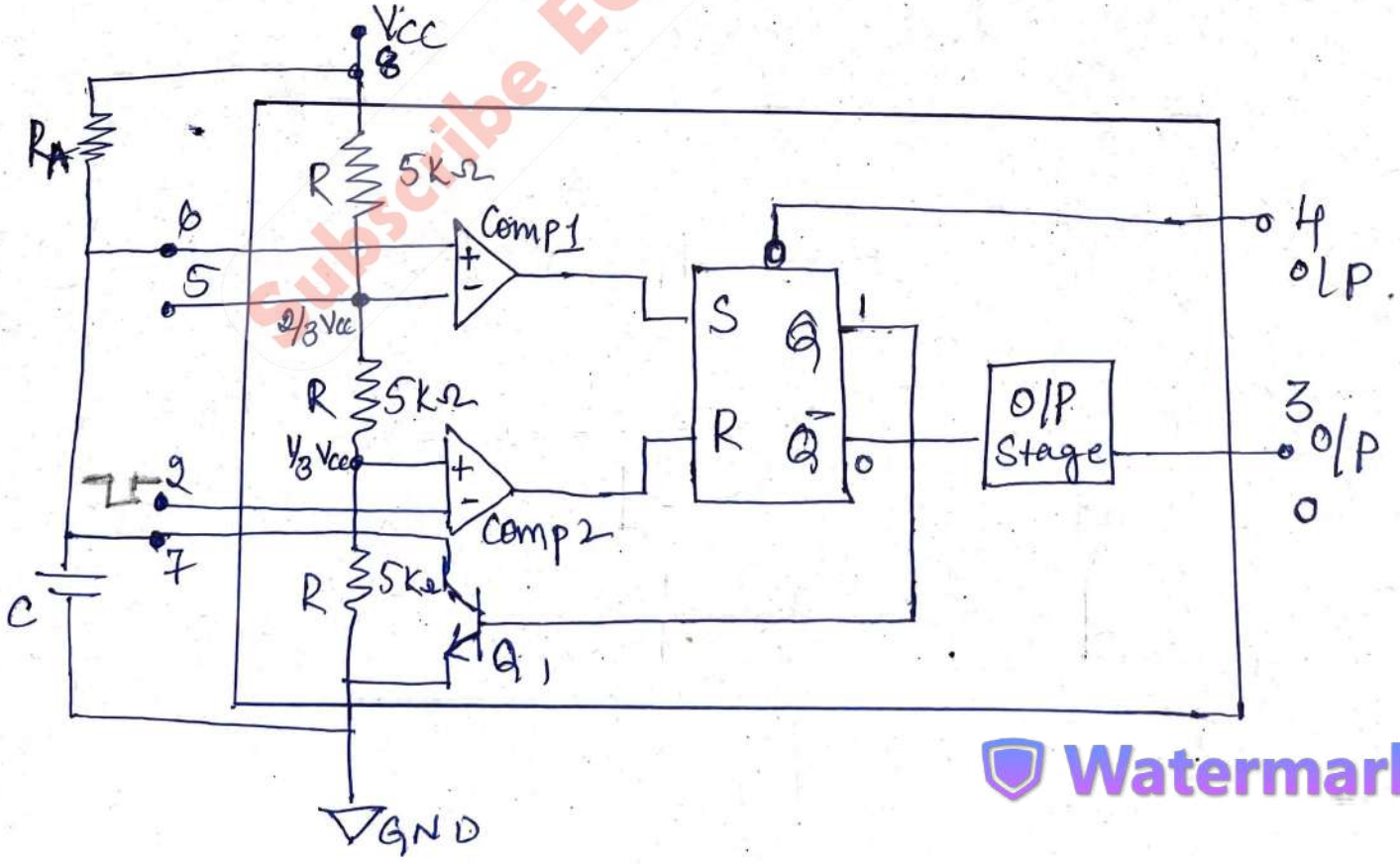
∴ ④ Freq of oscillation $f_o = 1/T = \frac{1.45}{(R_A + 2R_B) C}$

Monostable Multivibrator using 555

- One stable pulse.
- one shot Multivibrator.
- Needs external trigger pulse for o/p = 1 (high).
- else o/p remains low.







- Initially the o/p is low.

→ trigger pulse is applied a/c i/p of Comp 2 then $t_{ig} < \frac{1}{3} V_{cc}$.

- then the o/p of Comp 2 is high (Inverting Comparator)
- SR F.F. is reset then $Q = 0$ & $\bar{Q} = 1$
- 1 is the i/p to the o/p stage & the o/p will be high for some time

→ when $Q = 0$, will set transistor Q_1 to be off & act as open circuit

- then Capacitor starts Charging with Vcc.
- at pin no 6 i/p is equal to $V_{cc} > \frac{2}{3} V_{cc}$
- then the o/p of Comp 1 is high (non Inverting Comparator)
- SR F.F. is set then $Q = 1$ & $\bar{Q} = 0$
- Since $\bar{Q} = 0$ the o/p will be low.
- the capacitor starts discharging since Q_1 act as short Circuit.

o/p remains HIGH for $t_p = 1.1 R_A C$ sec.

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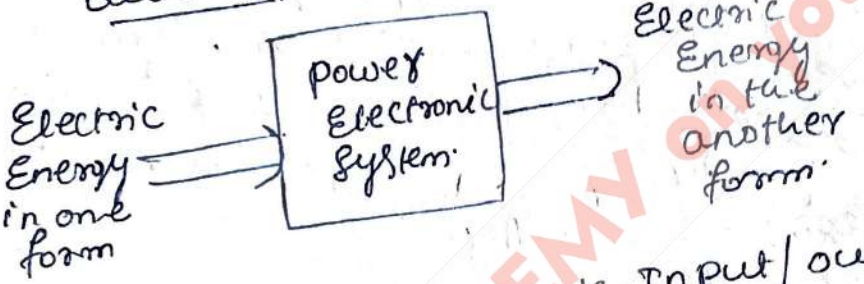
Module-5

Module 1 :

Introduction to Power Electronics

Power Electronics is one of the important branch of Electronics and Electrical Engineering. It deals with conversion and control of Electric Energy. We know that AC Voltage and Current of fixed frequency is available from mains. This supply cannot be ~~used~~ used always directly. for Example computer needs (Switch mode power supply) SMPS for its working.

Basic Inputs/outputs of power Electronic System



The above fig shows Basic Input/output of Power Electronic System. The Electric Energy in one form is given at the Input. The Power Electron System converts the Electric Energy in the other form. For Example, the Input may be AC & the o/p can be DC. we know that such conversio is performed by rectifier. Thus rectifier is a Power Electronic System.

The Power Electronic System thus performs conversion of Electric Energy. It also controls the amount of Electric Energy to be given to the output. The word power means high amplitude of current and voltages.

Brief History of Power Electronics

* The first power Electronics device developed was the mercury Arc Rectifier during the year 1900.
* The other power devices like metal tank rectifier, grid controlled vaccum tube rectifier, ignitron, Phanotron; thyratron and magnetic amplifier were developed & used gradually for power control application until 1950s.
* The first SCR (Silicon controlled Rectifier) or Thyristor was Invented & developed by Bell Lab's in 1956 which was first PNPN triggering transistor.
* The second Electronic revolution begin in the year 1958 with the development of commercial grade Thyristor by the general Electric company [GE]. Then the new Area of power Electronics was born.
* After that many different types of power Semiconductor devices & power conversion Technique have been Introduced.
* The power Electronics revolution is giving us the ability to convert, Shape & control large amount of power.

Block diagram of the generalized power system is shown in ~~above~~ Below.

Power source may be an ac supply system or a dc supply system. In India 1 phase and 3 phase 50 Hz ac supplies are readily available in most location. Very low power drives are generally fed from single phase (1φ) source. Rest of the drives are powered from 3 phase source.

power modulator : power modulator converts electrical energy of the source as per the requirement of the load. For example if the load is a dc motor, the modulator output must be adjustable direct voltage.

In case of load is 3 phase Induction motor, the modulator may have adjustable voltage & frequency at its output terminal. When power modulator performs this function, it is known as converter.

motor commonly used in power electronic system are

(1) DC motors (Shunt, Series, Compound and permanent magnet)

(2) Induction motors (Squirrel-cage, wound rotor & Linear)

(3) Synchronous motors (wound field and permanent magnet)

(4) Brushless DC motors.

(5) Stepper motors

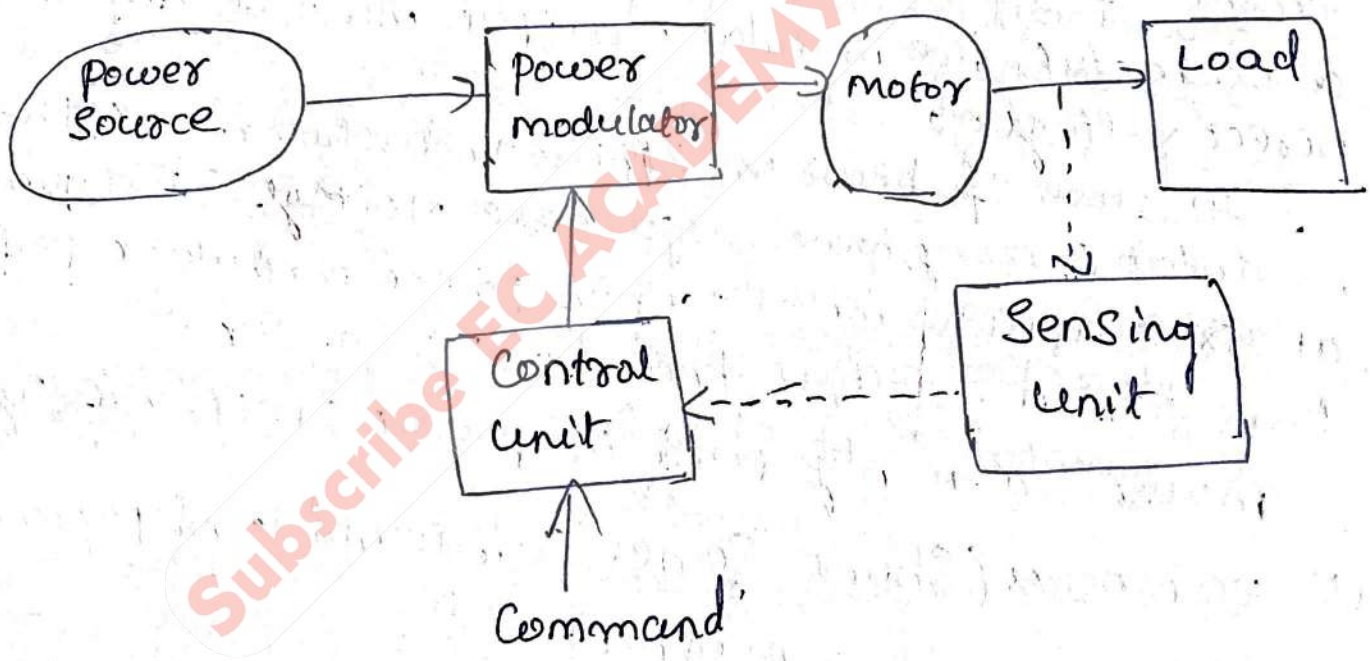
(6) Switched Reluctance motors.

Power modulators are controlled by a control unit. Nature of the control unit for a particular system depends on the power modulator that is used.

Control unit operates at much Lower voltage and power Levels.

Sensing unit measures the Load Parameters. Say speed in case of Rotating machine & compares it with the command.

Power Electronic System Block diagram



Types of power converters or Types of power Electronic circuits

For the control of electric power supplied to the load or the equipment/machinery or for power conditioning the conversion of electric power from one to other is necessary & the switching characteristic of power semiconductor devices (Thyristors) facilitate these conversions.

The different types of power converters are

(1) Phase controlled Rectifiers (AC to DC converters).
(2) Choppers (DC to DC converters)
(3) Inverters (DC to AC converter.)
(4) Cycloconverters (AC to DC converters)
(5) AC voltage controllers (AC Regulators).

(1) Power controlled Rectifiers (AC to DC converters)

These controllers convert fixed ac voltage to a variable dc output voltage. These converters takes power from one or more ac voltage/current sources of single or multiple phases and delivers to a load. The output variable is a low ripple dc voltage or dc current. These controller circuits use line voltage for their commutation. hence they are also called as line commutated or naturally commutated ac to dc converters. These circuit include diode Rectifiers and Single/Three Phase controlled circuits.

Applications:-

(1) High voltage dc Transmission Systems.
(2) Dc motor drives.
(3) Regulated Dc power Supplies
(4) Static VAR compensator.
(5) Battery charger circuits.
(6) wind generator convertors.

(2) Choppers (DC to DC converters)

A chopper converts fixed dc Input voltage to a variable dc output voltage. The dc output voltage may be different in amplitude than the Input Source voltage. choppers are designed using Semiconductor devices such as power transistor, IGBTs, GTO, Power MOSFET & Thyristors. output voltage can be varied steplessly by controlling the duty ratio of the device by Low power Signals from a control unit. chopper has Either a Battery, a Solar powered dc voltage Source or Line frequency (50-60Hz) derived dc voltage Source.

Applications: Dc Drives
Battery driven vehicles
Electric traction.
Switched mode Power Supplies
Subway Cars.

(3) Inverters (DC to AC converters)

An Inverter converts a fixed DC voltage to an AC voltage of variable frequency & of fixed or variable magnitude. A practical Inverter has either a battery, a Solar powered dc voltage Source or a Line frequency (50Hz.) derived dc voltage Source. Inverters are widely used from very Low power portable electronic Systems such as flashlight discharge System in a Photography Camera to very high power Industrial Systems.

Inverters are designed using Semiconductor devices such as power transistor, MOSFETS, IGBTS GTO and Thyristor.

Application:

(1) Uninterrupted Power Supply (UPS)
(2) Aircraft and Space Power Supplies.
(3) Induction & Synchronous motor drives.
(4) High voltage dc Transmission System.
(5) Induction Heating Supplies

(4) Cycloconverters (AC to AC Converters)

These circuits convert Input Power at one frequency to output power at a different frequency through one Stage conversions. These are designed using Thyristors and are controlled by Triggering Signals derived from a control unit.

The output frequency is Lower than the source frequency. output frequency in Cyclo converter is a simple fraction such as $\frac{1}{3}$ $\frac{1}{5}$ and so on of the source frequency.

These are mainly used for Slow Speed very high power Industrial drives.

Applications: Ac drives like Rotary kilns multi-mw ac motor drives.

5) AC Voltage Controllers (AC Regulators):

These converters convert fixed ac voltage directly to a variable ac voltage at the same frequency using Line Commutation.

These converters Employs a Thyristorised voltage controller.

Applications: Lighting Control
Speed control of large fans & pumps.
Electronic tap changers.

Power Electronic Applications

(1) Home appliances: Refrigerators, Sewing machines, photography, Airconditioning, food warming trays, washing machines, Lighting dryers, Vaccum cleaners, grinders and mixers.

(2) Games and Entertainment
Games and Toys, Televisions, movie Projectors.

(3) Commercial:
Advertising, Battery chargers, blenders, computers, Electric fans, Electronic ballasts, hand Power tools; vending machines

(4) Aerospace:
Aircraft power System, Space vehicle Power Systems, Satellite power Systems.

(5) Automotive:
Alarms & Security Systems, Electric Vehicles, audio and RF amplifiers, Regulator.

(6) Industrial:
Elevators, UPS, welding Equipment, ultrasonic generators, power supplies, printing press, machine tools, Electric vehicles, Electromagnet, Electronic ignitions, ovens, Electric furnaces etc

(7) medical :
Fitness machines, Laser power Supplies, medical Instrumentation.

(8) Security System
Alarms and Security System, radar/Sonar.

9) Telecommunication
uninterruptible power Supplies (UPS), Solar power Supplies, wireless communication power Supplies

10) Transportation
magnetic Levitation trains & Locomotives, motor drives,

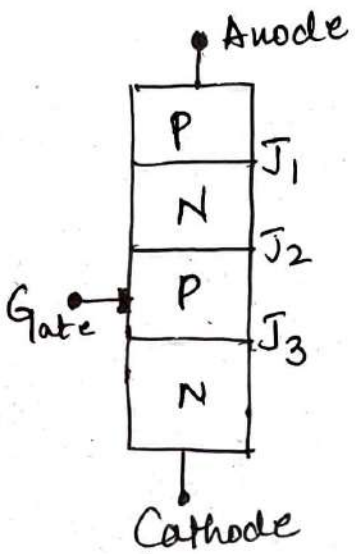
11) Utility System : VAR Compensators, power factor correction, Static Circuit Breakers.

SCR (Silicon Controlled Rectifier)

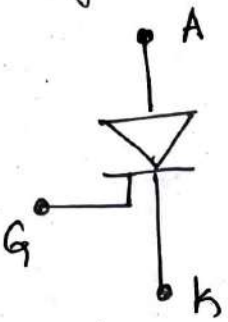
→ Silicon Semiconductor material.

→ Control → AC to DC Conversion.

Construction



Symbol

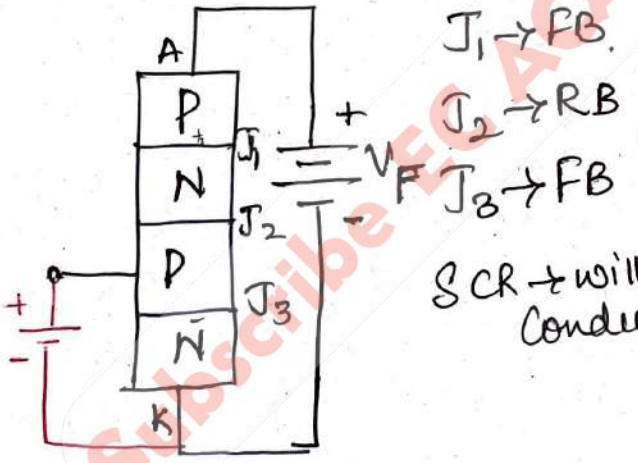


Working :-

1. Forward blocking Mode
2. Forward Conduction Mode
3. Reverse blocking Mode.

J_1, J_2, J_3 } → FB → Forward Conduction of SCR

1. Forward blocking Mode

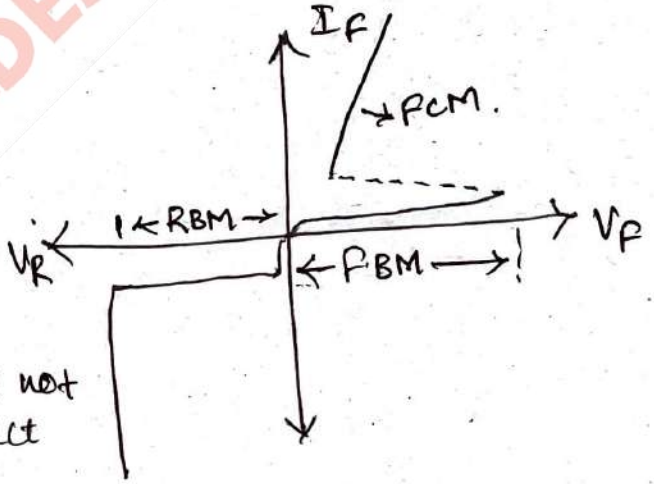


J_1 → FB.

J_2 → RB

J_3 → FB

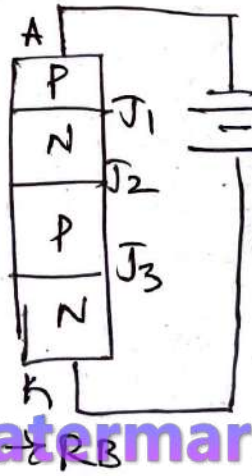
SCR → will not Conduct



2. Forward Conduction mode.

J_1, J_2, J_3 } FB → SCR starts Conducting.

3. Reverse blocking mode



J_1 → RB

J_2 → FB

J_3 → RB

SCR → RB

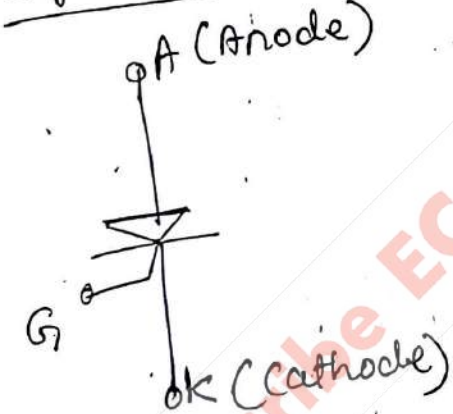
Thyristor:

Thyristor is a general name given to a family of power semiconductor switching devices, all of which are characterised by a Bistable switching action depending upon the PNPN regenerative feedback. The Thyristor has 4 or more Layers and Three or more Junctions.

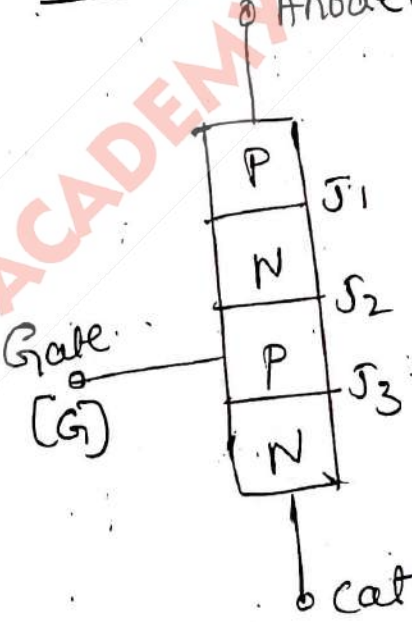
The SCR [Silicon controlled Rectifier] is the most widely used and Important member of the Thyristor family.

PRINCIPLE OF operation of SCR

Symbol



(Structure



The Structure and Symbol of the Thyristor [SCR] is shown in above diagram. It is a Four Layered PNPN switching device, having Three Junctions J1, J2, & J3. It has three External terminals namely Canode (A) Cathode (K) and gate (G). The anode and cathode are connected to the main power circuit. The

gate terminal carries a low level gate current in the direction gate to cathode. Normally the gate terminal is provided at the P-Layer near the cathode.

operation:- when anode is made positive with respect to cathode, The junctions J_1 & J_3 are forward biased but the middle junction J_2 becomes Reverse biased. Thus the junction J_2 because of the presence of depletion Layer, does not allow any current to flow through the device. only leakage current, negligibly small in magnitude, flows through the device due to the drift of the mobile charges. This current is Insufficient to make the device Conduct. In other words, the SCR under the forward biased condition does not conduct. This is called as the forward Blocking State OR off State of the device.

when Anode to cathode voltage Increases, the width of the depletion Layer at the junction J_2 decreases.

If again anode to cathode voltage is kept at a stage comes when the depletion Layer at J_2 vanishes. The reverse biased Junction J_2 will Breakdown due to the Large voltage produced across its depletion Layer. This Phenomenon is known as the Avalanche Breakdown.

Since the other junctions J_1 and J_3 are already forward biased, there will be a free carrier movement across all the three junctions resulting in a large amount of current flowing through the device from anode to cathode. Due to the flow of this forward current, the device starts conducting & it is then said to be in the conducting state or ON state.

When Anode is made negative with respect to cathode [cathode is positive], The junction J_1 & J_3 are Reverse biased & the junction J_2 become Forward biased.

Thus the junctions J_1 & J_3 do not allow any current through the device. only a very small amount of leakage current may flow because of the drift of the charges, the leakage current is again insufficient to make the device conduct. This is known as the Reverse Blocking state or Off state of the device.

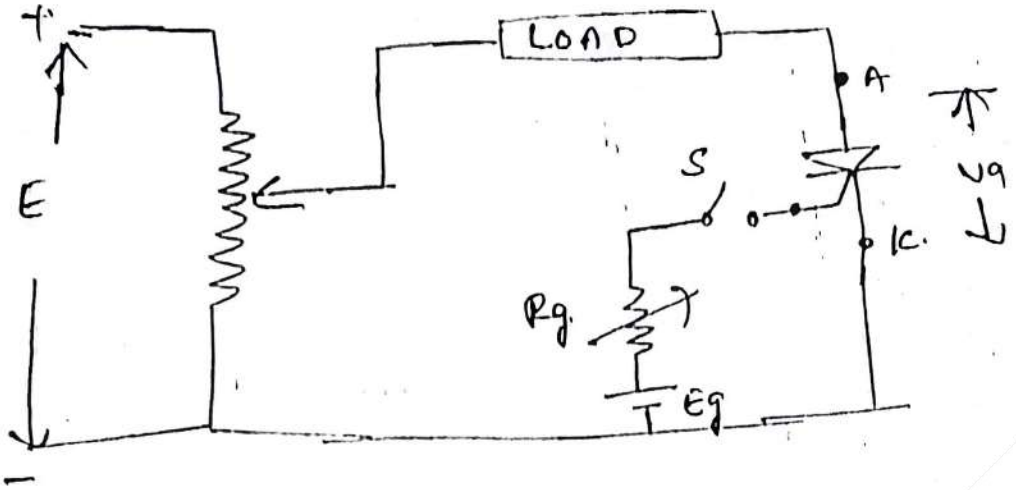
The different Types of Thyristors are

(1) SCR [Silicon Controlled Rectifier]

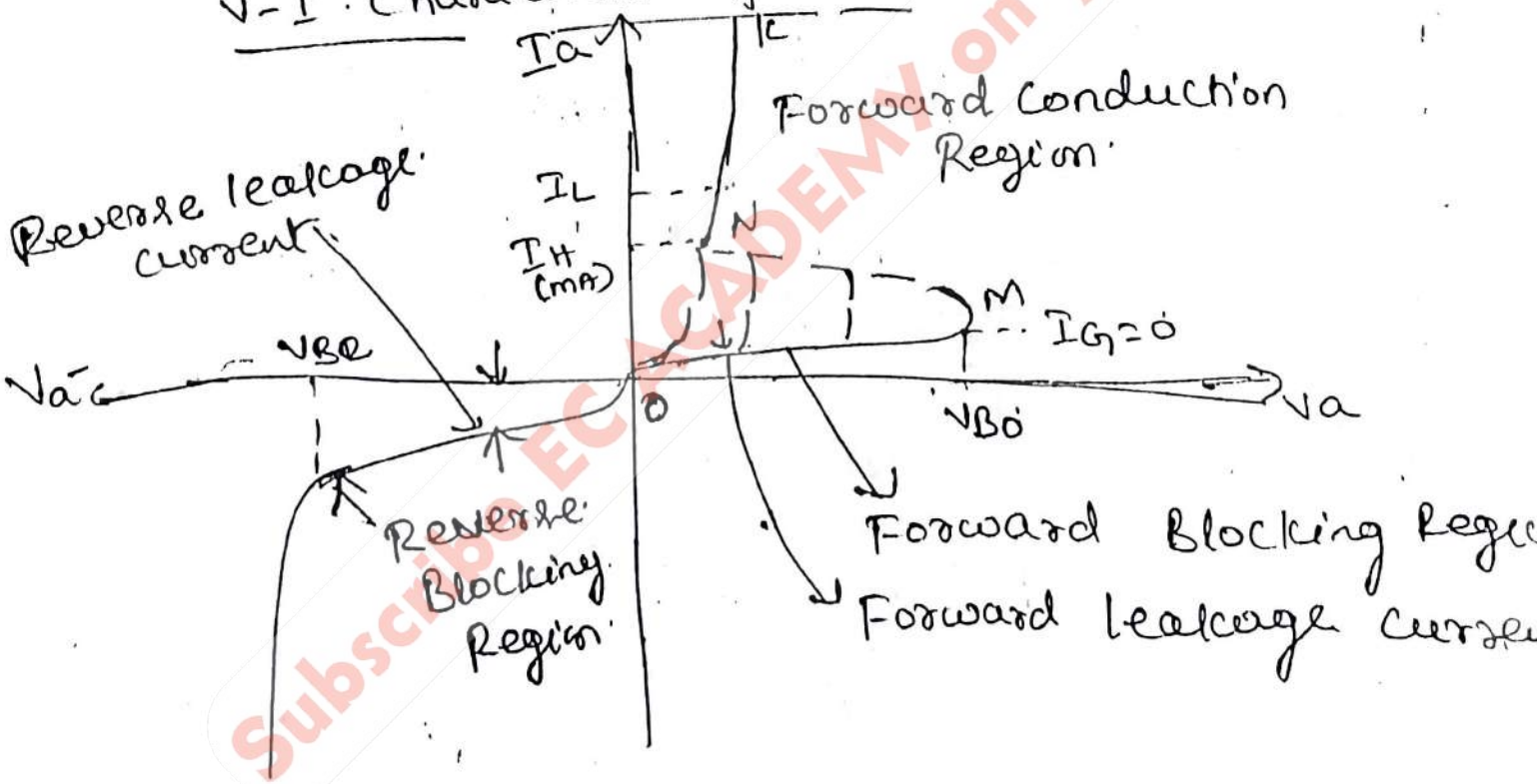
(2) TRIAC

(3) DIAC (4) GATE TURN OFF THYRISTOR [GTO]

Static anode - cathode characteristics of SCR



V-I Characteristic of SCR



V_{BO} → Forward breakover voltage.

I_L → Latching Current, I_H → Holding Current

V_{BR} ⇒ Reverse Breakover voltage.

I_G = Gate Current

Static anode-cathode characteristic of SCR can be classified into 3 Region.

(1) Forward Blocking Region
(2) Forward Conduction Region.
(3) Reverse Blocking Region

(1) Forward Blocking Region

In this Region, the anode is made positive with respect to the cathode & therefore Junction J_1 & J_3 are forward biased while the Junction J_2 Remains Reverse biased. Hence the anode current is a small forward leakage current. The Region om of the V-I characteristic is known as the forward blocking region when the device does not conduct.

(2) Forward Conduction Region

When the anode to cathode forward voltage is Increased with gate Circuit kept open, avalanx Breakdown occurs at the Junction J_2 at a Critical forward Break over voltage (V_{BO}) & SCR Switches into a Low Impedance condition. forward Breakover voltage is corresponding to the point m, when the device [illegible]

to the conducting State.

The Region MN of the characteristic shows that as soon as the device Latches on to it's ON State; the voltage across the device drops from say, several hundred volts to 1-2 volt. depending on the rating of the SCR. & Suddenly a very large amount of current starts flowing through the device. The part NK of the characteristic is called as the forward conduction State.

The anode current must be more than a value known as Latching current I_L.

Latching current I_L is the minimum anode current required to maintain the Thyristor in the ON-State Immediately after a Thyristor has been turned on & the gate signal has been removed

If the forward anode current is reduced below a level known as the holding current I_H. Holding current I_H is the minimum anode current to maintain the Thyristor in the on-State.

The holding current is in the order of milliampere & is less than the Latching current I_L.

3) Reverse Blocking Region:

When the Cathode is made positive with respect to anode with the Switch S open, the Thyristor becomes reverse biased.

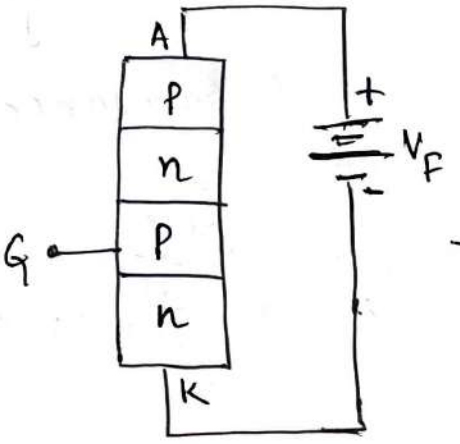
In fig OP is the Reverse blocking Region, In this Region, the Thyristor Exhibits a Blocking Characteristic Similar to that of a diode.

In this reverse biased condition, the junction J1 & J3 are Reverse biased & the middle junction J2 is Forward biased. Therefore, only a Small leakage current (in mA) flows. If the reverse voltage is Increased, then at a Critical Breakdown Level called reverse Breakdown Voltage V_{BR}.

SCR Turn ON methods :-

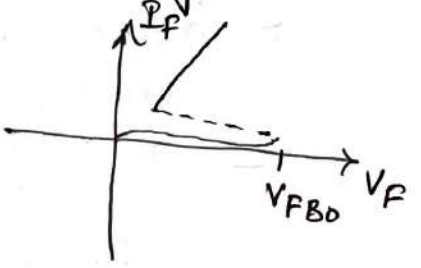
1) Forward Voltage Triggering
2) Gate Triggering
3) dV/dt Triggering
4) Light Triggering
5) temparature Triggering.

1) Foward Vtg Triggering



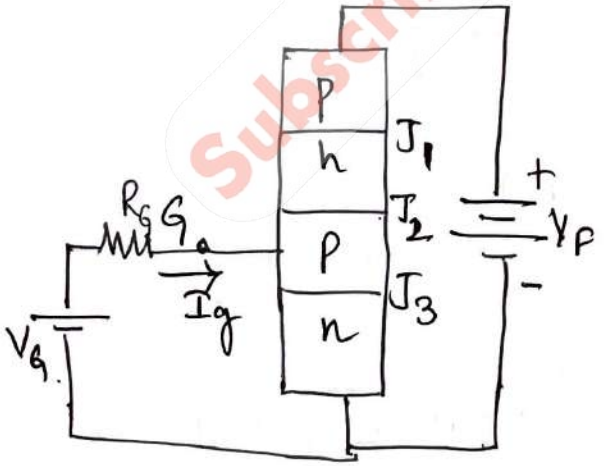
→ SCR is Forward biased and no. Vtg is applied accross the gate.

→ As forward Vtg increases beyond forward break down (V_{FBO}) the SCR starts conducting.



→ This method is very less used.

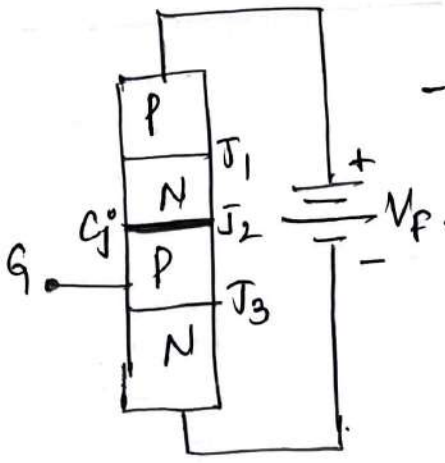
2) Gate Triggering



→ Along with forward biasing the SCR, the Gate Vtg is applied.

→ due to this Junction J_2 is Forward biased and SCR will turn ON.

3) dV/dt triggering :-



- When SCR is Forward biased
- Junction J_1, J_3 is Forward biased
- J_2 → reverse biased hence it will act as a Capacitor (C_j)
- C_j will store the charges.

$q = C_j \cdot V_a$ $\quad C_j$ → junction Capacitance, V_a → anode V+e

$\frac{dq}{dt} = i_j = C_j \cdot \frac{dV_a}{dt} + V_a \cdot \frac{dC_j}{dt}$ (neglect this term)

$$\boxed{i_j = C_j \cdot \frac{dV_a}{dt}}$$

- here as V_a increased i_j will also increase
- if i_j increases it will break the depletion region across J_3
- The SCR Starts Conducting.

4) Light Triggering (LASCR)

- here we will use light activated SCR.
- A light is passed through the gate terminal
- that will break the junction across J_3
- SCR Starts Conducting.

5) Temparature Triggering

- when temp is provided across the gate
- Junction breakdown occurs & SCR Starts Conducting

SCR Turn OFF methods :-

1) Natural Commutation.
2) Reverse bias Turn OFF
3) Gate Turn OFF.

1) Natural Commutation.

- Once the SCR is ON and if the Gate Vtg is removed even then the SCR will remain ON
- If anode current is reduced less than Holding Current.
- SCR will turn OFF.

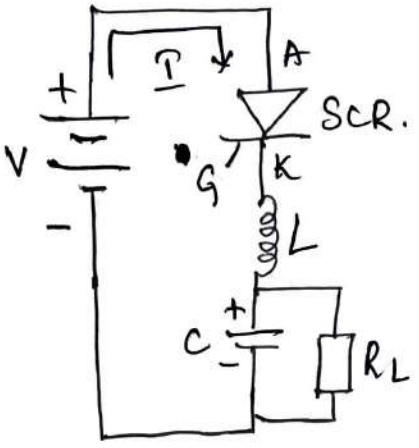
2) Reverse bias.

- If Rverse bias is applied accross the SCR
- SCR will turn OFF.

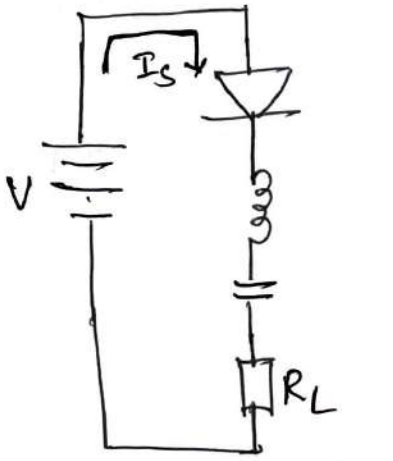
3) Gate Turn OFF :-

- If negative Vtg is applied accross the Gate.
- The negative gate current, holding Current increased and SCR will turn OFF.

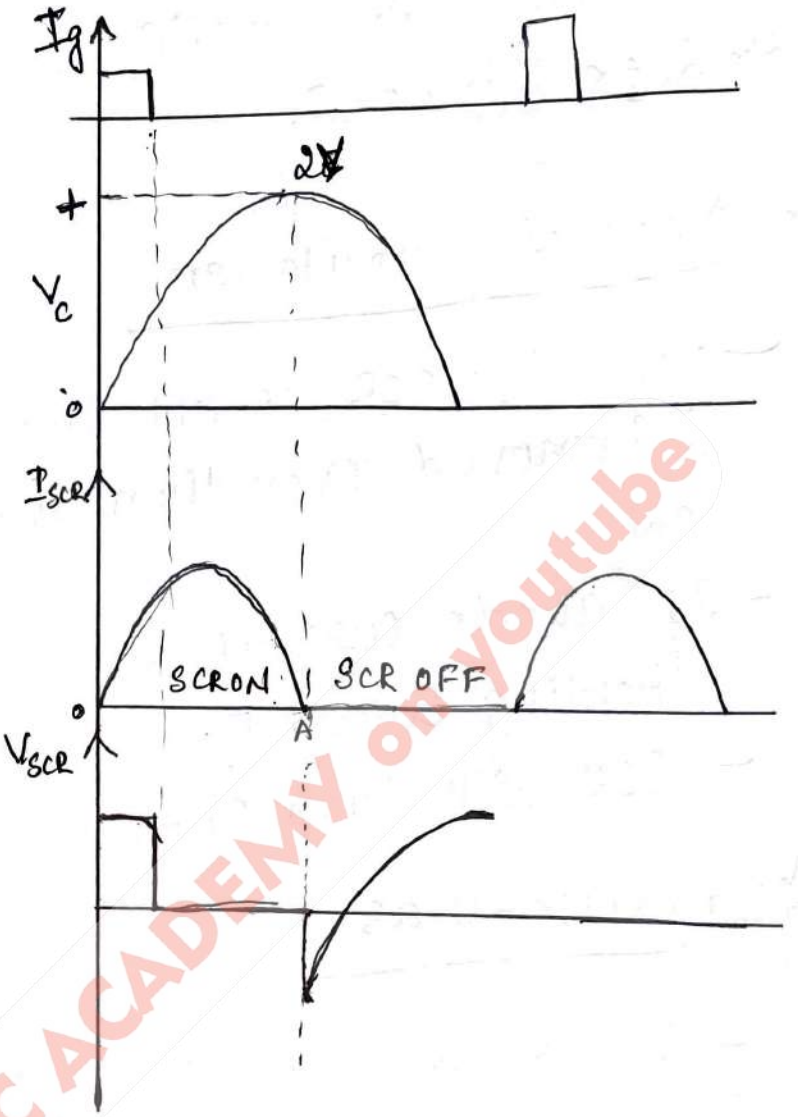
Forced Commutation - class A (Self commutation)



R_L high.



R_L value low



- RLC is used to turn OFF SCR.
- when gate pulse is applied SCR is ON.
- L & C starts charging.
- L provides reverse current to SCR.
- hence SCR current decreases and SCR is turned OFF.
- Once

Firing Circuits of SCR :- (Gate Trigger Circuits) (21)

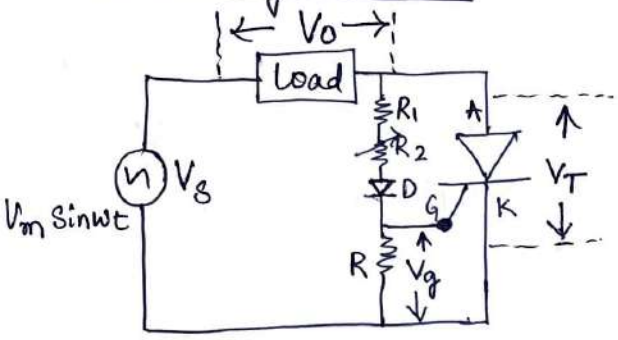
→ used to turn ON SCR.
↳ we can turn on the SCR at desired instant of time.

a) R - Firing (Resistance) circuit
b) RC - Firing (Resistance - Capacitance) circuit
c) UJT - Firing circuit.

→ Some of the commonly used Firing Ckts are named above.

→ A control Ckt is used b/w Gate and Cathode to turn on the SCR
→ These control Ckts are known as Firing Ckts (or) Triggering Ckt

R - Firing Circuit :



→ Fig. shows a half wave Controlled rectifier Ckt
→ Vs, load and SCR is connected in series.
→ Ckt Connected b/w A & K is known as power Ckts because A & K can handle high Vtg & high current.
→ Ckt Connected b/w G & K is known as control Ckts which are low power Ckts
→ R-firing Ckts are simplest & most economical Ckts
→ The resistor R_1 limits the current through the gate of the SCR
→ R_2 is the variable resistor, by varying the resistance we can control the firing angle (α) of SCR
→ Hence it is known as R-firing Ckt.
→ R is the stabilizing resistor
→ Diode ensures that no negative Vtg reaches the gate of SCR. * Diode allows current only in +ve half cycle only

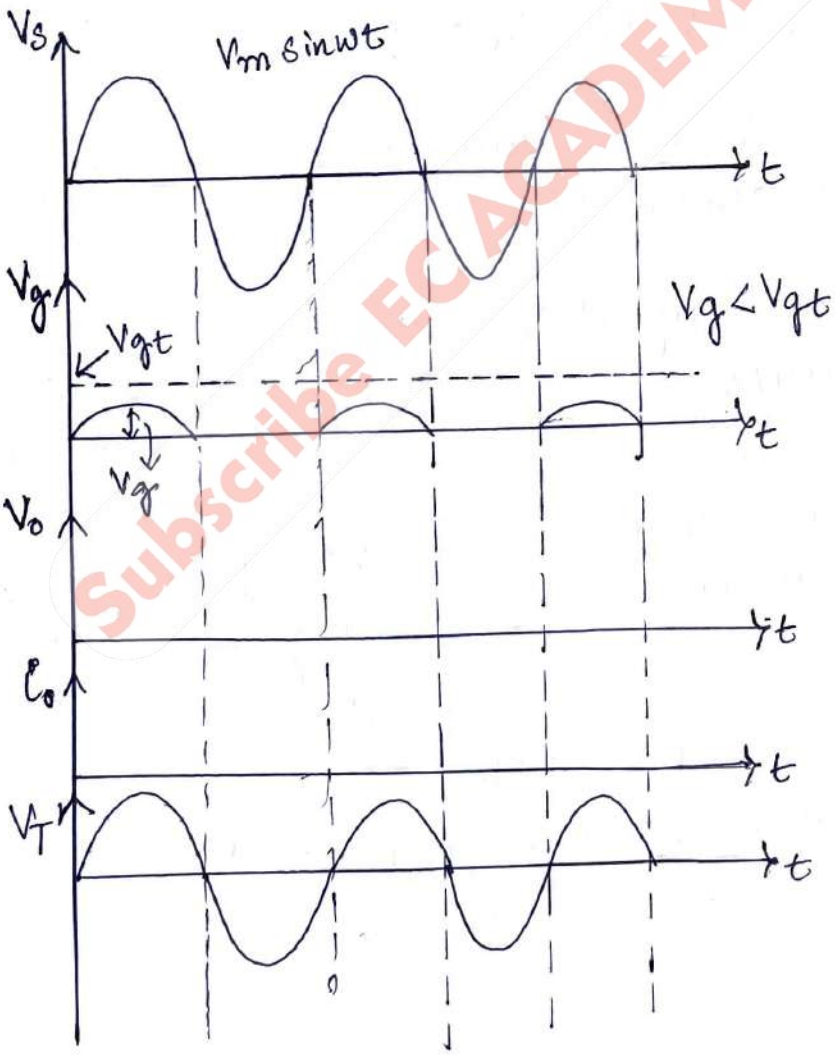
Operation :-

→ Initially SCR is in OFF state
→ Apply the supply Vtg

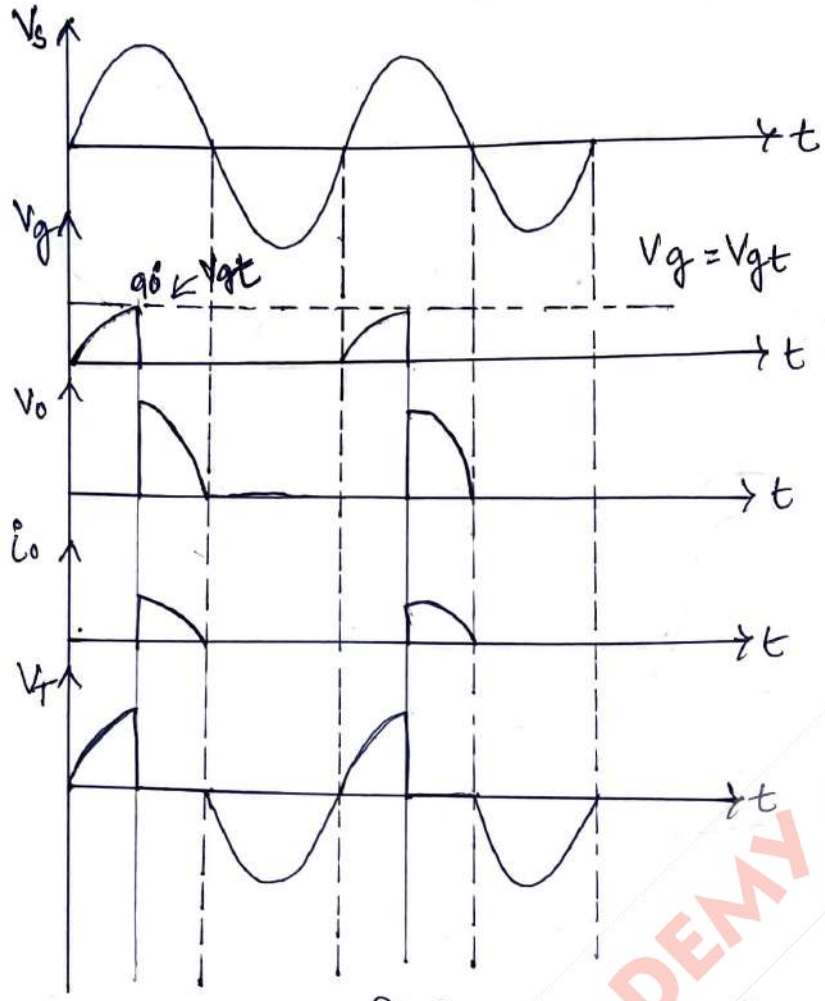
→ During the half cycle Anode is +ve & Cathode is negative
→ Dute to this J_1 & J_3 is Forward biased but J_2 is reverse biased condition.
→ SCR will be OFF ⇒ It will act as open switch.
→ Current will flow from V_s, load, R_1, R_2 R & back to Source. (V_s)
→ $V_g = V_{gt}$ (Gate trigger V_{tg}) – SCR will turn ON
→ Then current flows from V_s, SCR & back to V_s
→ During -ve half of i/p SCR will be OFF.

Case(i): when R_2 is very large.

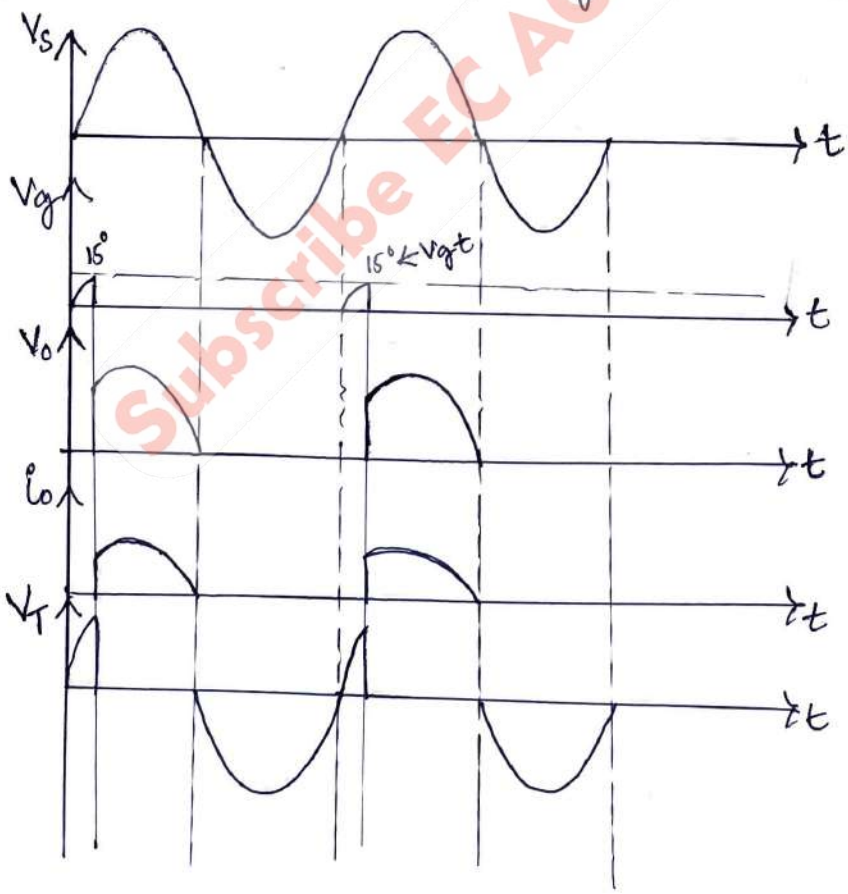
→ The current through resistors will be very less
→ Hence $V_g < V_{gt}$ ⇒ SCR will be OFF



Case(ii) when R_2 is optimum.



Case (iii) when R_2 is very Small.



→ Firing angle (α) depends on Value of R_2

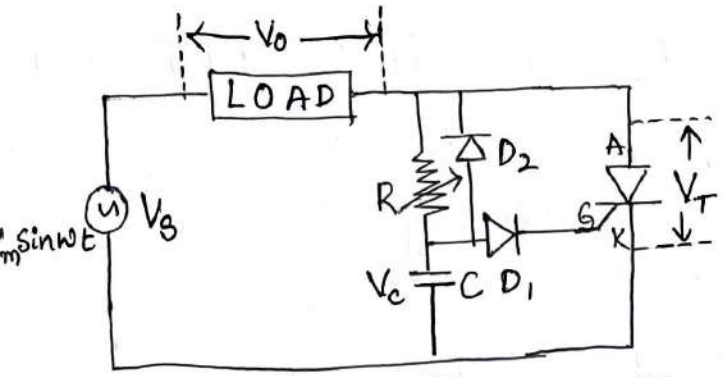
→ $\alpha \propto R_2$

→ α ranges from (0 to 90°) can not be upto 180° (Limitation)

– To overcome this limitation we will use RC & UJT Firing Ckts.

RC Firing circuit :-

→ RC Half wave triggering ckt
→ RC full wave triggering ckt

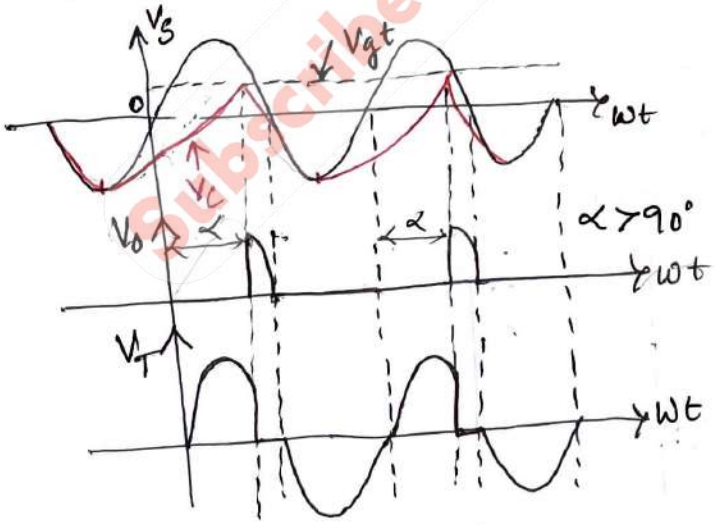


(i) Half wave Triggering ckt

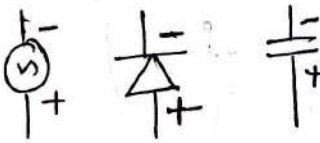
- R firing ckt can provide the firing angle (α) from 0° to 90°
- to over come this limitation RC firing ckt is used.

- Fig shows the RC triggering ckt
- Ckt b/w A & K is power ckt
- Ckt b/w G & K is control ckt
- Control ckt consists of two diodes D_1 & D_2, Variable resistor R & a Capacitor.
- by varying the resistor value of R we can control the firing angle from 0° to 180°

Operation :- (i) R is large



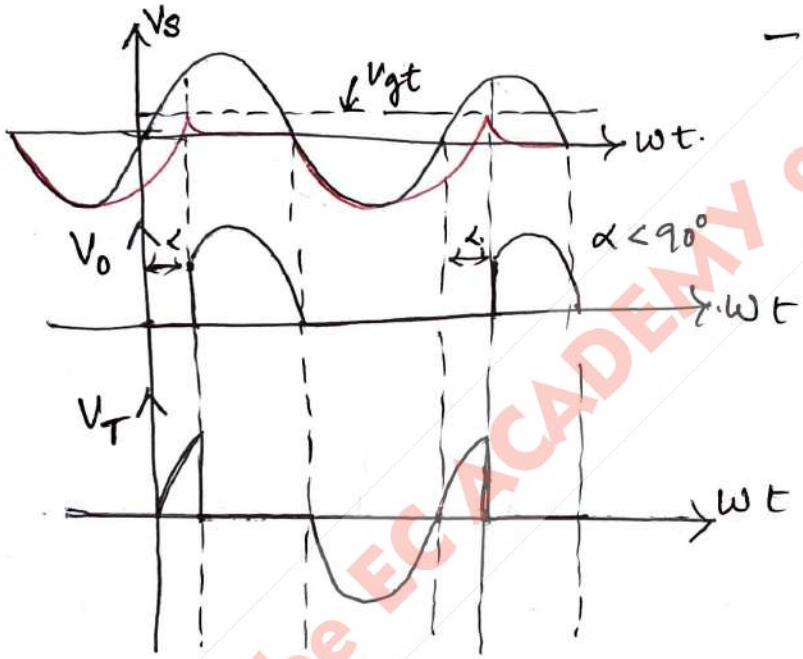
- During -ve half of i/p Diode D_2 is forward biased and current flows from V_s, through Capacitor C, Diode D_2 & back to source V_s.



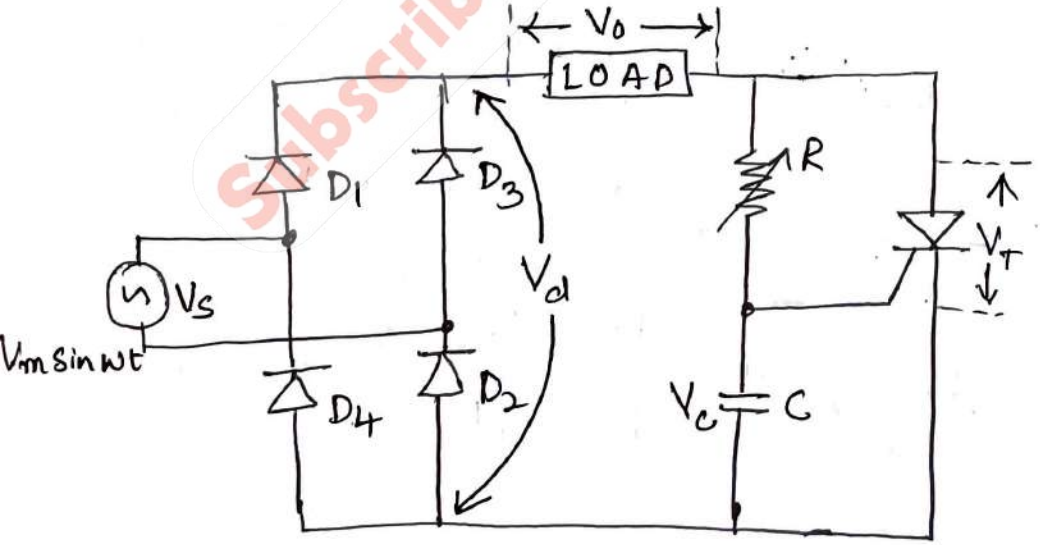
- So Capacitor C charges through diode D with [lower plate +ve & upper plate -ve] negative V_{tg}
- As the i/p V_{tg} moves towards +ve Peak the Capacitor will start charging with +ve V_{tg}

- As Capacitor V_{+g} reaches V_{gt} then SCR starts Conducting.
- Again During -ve half cycle i/p SCR will be OFF and during the half of i/p when $V_c = V_{gt}$ the SCR is ON & starts Conducting.
- When R is high then the Capacitor Charging time will also be more.

(ii) R is small

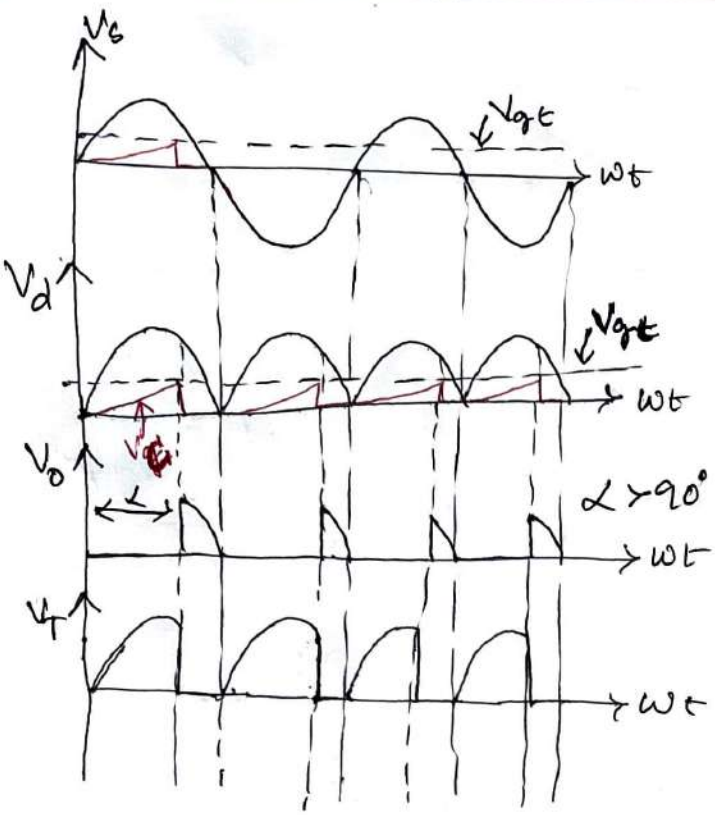


- If R value is less then Charging time of Capacitor is less.

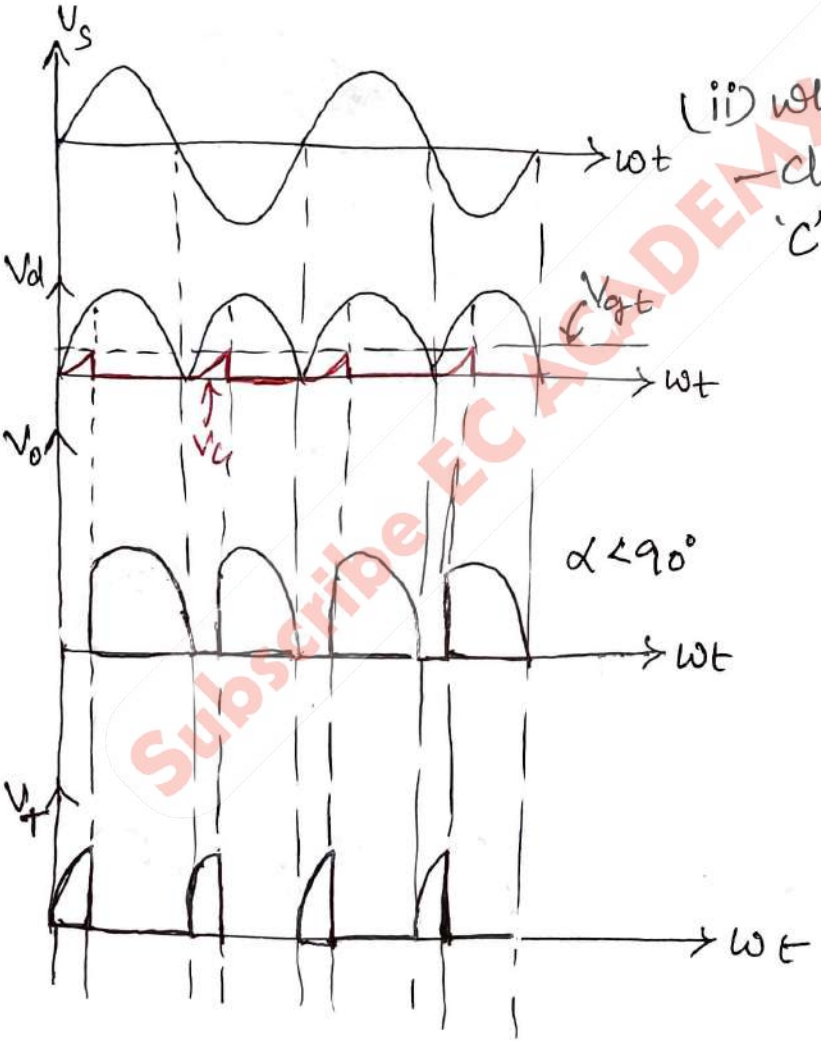


(ii) Full wave Triggering Ckt

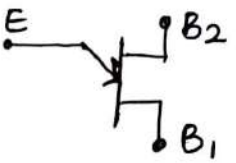
(i) When R is large
- charging time of capacitor 'C' is more.



(ii) When R is small
- charging time of capacitor 'C' is less.

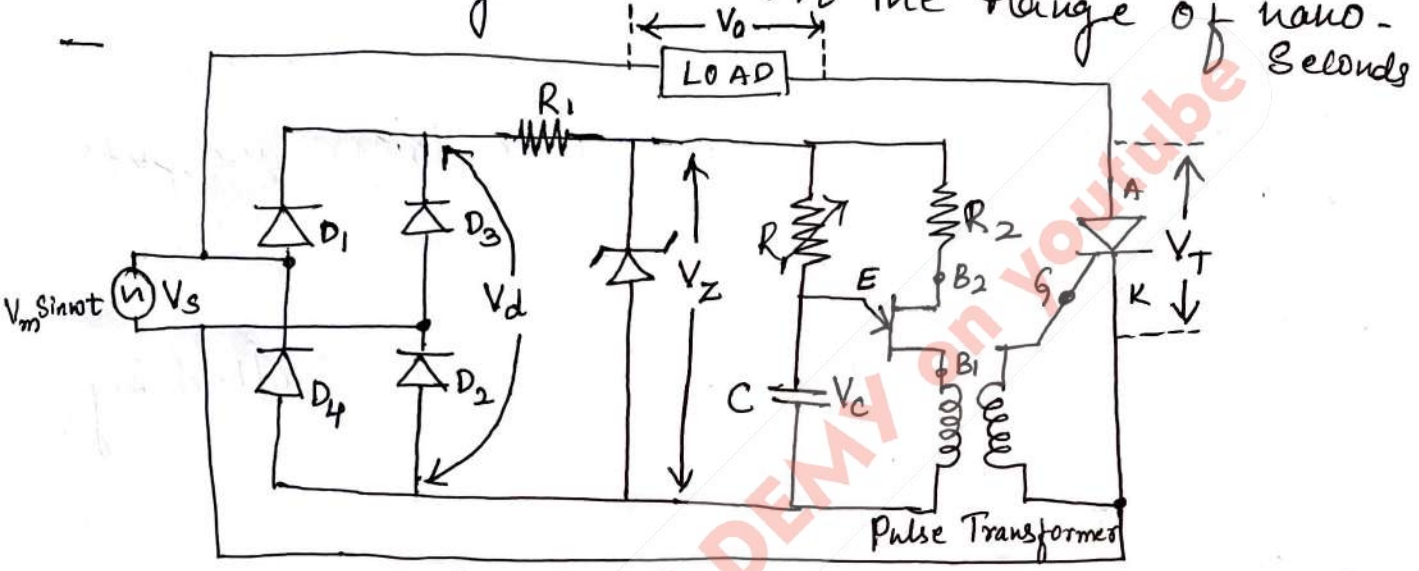


UJT Triggering Circuit :-



UJT ⇒ Unijunction Transistor

- It is an electronic Semiconductor device which has only one Junction
- It has 3 terminals Emitter, Base1 & Base2.
- It is a highly Efficient Switch.
- Its Switching time is in the range of nano-seconds



- Fig. shows the UJT Triggering circuit.
- Ckt b/w A & K is Power Circuit
- Ckt b/w G & K is Control circuit.
- V_s is applied to the bridge rectifier.
- Then the rectified Vtg V_d is applied to the Zener diode
- Zener diode will act as Voltage Regulator
- It will clip the Vtg V_d to a fixed Vtg V_z.
- V_z is applied to the Charging Ckt
- Capacitor C Charges through Resistor R_1

- When V_c reaches ~~Vota~~ UJT triggering V_{trg} (V_p)
- the UJT will turn ON.
- Capacitor will discharge through ~~primary of~~ Emitter, B_1 and primary of pulse transformer
- A pulse is produced at primary & secondary of pulse transformer
- This pulse will act as gate triggering pulse of SCR.
- Charging of Capacitor can be controlled by Varying Resistor R_1
- Hence firing angle can be controlled from 0° to 180°